MICRO-EPSILON

Operating Instructions

IF2008 ETH

Interface module

MICRO-EPSILON MESSTECHNIK
GmbH & Co. KG
Koenigbacher Str. 15

94496 Ortenburg / Germany

Tel. +49 (0) 8542 / 168-0
Fax +49 (0) 8542 / 168-90
e-mail info@micro-epsilon.com
www.micro-epsilon.com

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1. Safety

System operation assumes knowledge of the operating instructions.

1.1 Symbols Used

The following symbols are used in these operating instructions.

⚠ CAUTION	Indicates a hazardous situation which, if not avoided, may result in minor or moderate injury.
NOTICE	Indicates a situation that may result in property damage if not avoided.
➪	Indicates a user action.
i	Indicates a tip for users.
Measurement	Indicates hardware or a software button/menu.

1.1 Warnings

⚠ CAUTION

Connect the power supply and the display / output device according to the safety regulations for electrical equipment.

> Risk of injury

> Damage to or destruction of the interface module.

The supply voltage must not exceed the specified limits.

> Risk of injury

> Damage to or destruction of the interface module.

NOTICE

Avoid shocks and impacts to the interface module.

> Damage to or destruction of the interface module.

1.2 Notes on CE Marking

The following apply to the IF2008 ETH interface module:

- EU Directive 2014/30/EU
- EU Directive 2011/65/EU, “RoHS” Category 11

Products which carry the CE mark satisfy the requirements of the EU directives cited and the European harmonized standards (EN) listed therein. The EU Declaration of Conformity is available to the responsible authorities according to EU Directive, article 10, at:

MICRO-EPSILON MESSTECHNIK
GmbH & Co. KG
Koenigbacher Str. 15
94496 Ortenburg / Germany

The measurement system is designed for use in industrial environments and meets the requirements.

1.2 Intended Use

- The IF2008 ETH interface module is designed for use in industrial and laboratory applications. It is used to convert the MICRO-EPSILON internal sensor protocol (RS422) to Ethernet.
- The IF2008 ETH interface module must only be operated within the limits specified in the technical data, see 2.
- The IF2008 ETH interface module must be used in such a way that no persons are endangered or machines and other material goods are damaged in the event of malfunction or total failure of the controller.
- Take additional precautions for safety and damage prevention in case of safety-related applications.

1.3 Proper Environment

Protection class: IP 65

Temperature range:

- Operation: 0 ... +50 °C (+32 ... +122 °F)
- Storage: +5 ... +50 °C (+41 ... +122 °F)

Humidity: 5 - 95 % (non-condensing)

Ambient pressure: Atmospheric pressure

2. Technical Data

2.1 Mechanics and Environment

Temperature range:

- Operation: 0 ... +50 °C (+32 ... +122 °F)
- Storage: +5 ... +50 °C (+41 ... +122 °F)

Protection class: IP 65 (When all plugs are connected.)

Dimensions: Interface module approx. 220 x 171 x 29, 1 mm
(outer dimensions incl. mounting brackets and connectors)

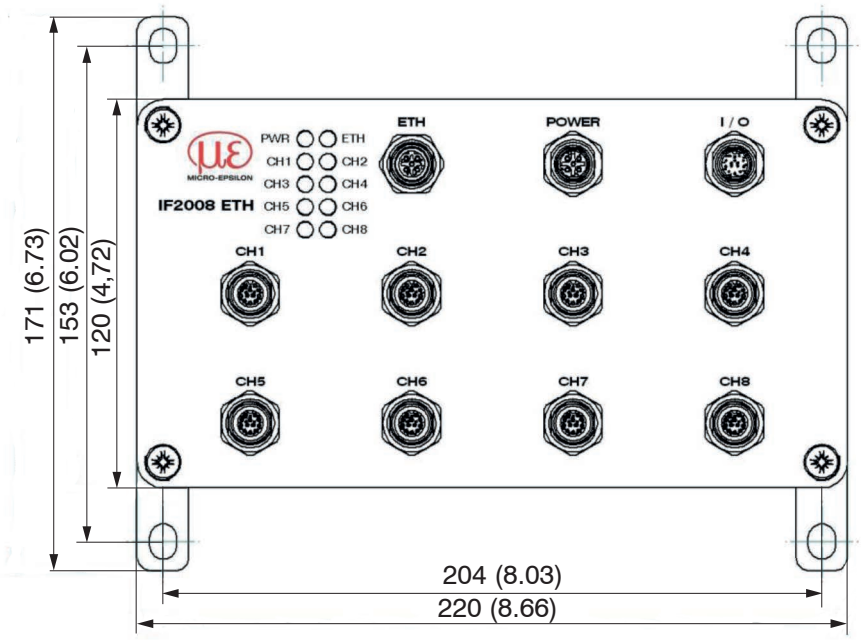


Fig. 1 Dimensional drawing for IF2008 ETH interface module in mm, not to scale

- Connections:
  - 1 flange socket, 4-pin, type Binder 09 3732 500 04 for Ethernet connection
  - 1 flange connector, 5-pin, type Binder 09 3441 600 05 for power connection
  - 1 flange connector, 12-pin, type Binder 09 3491 600 12 for I/O
  - 8 flange sockets, 12-pin, type Binder 09 3492 600 12 (channels 1-8) for sensor/encoder connection
- Status LEDs:
  - 1 LED for power status
  - 1 LED for Ethernet status
  - 8 LEDs for sensor/encoder status

2.2 Power Supply

- 11 - 30 VDC power supply for interface module and sensors
- Reverse polarity protection: yes
- Galvanic isolation: no
  All GND signals are connected internally and with the housing.

2.3 Ethernet

- LAN interface 100 Mbit

2.4 Sensor/Encoder Interface

- The following sensor types can be connected:
  - ILD 1420
  - ILD 2300
  - IFC 2451 / IFC 2461 / IFC 2471
- The following encoder types can be connected:
  - Power supply +5 VDC
  - RS422 interface with quadrature signals and reference mark

3. Delivery

3.1 Unpacking, Included in Delivery

1 IF2008 ETH interface module

1 Operating instructions

➪ Carefully remove the components of the measuring system from the packaging and ensure that the goods are forwarded in such a way that no damage can occur.

➪ Check the delivery for completeness and shipping damage immediately after unpacking.

➪ If there is damage or parts are missing, immediately contact the manufacturer or supplier.

Optional accessories are available in the appendix, see A 1.

3.2 Storage

- Temperature range storage: +5 ... +50 °C (+41 ... +122 °F)
- Humidity: 5 - 95 % (non-condensing)

4. Hardware

4.1 Connector Overview

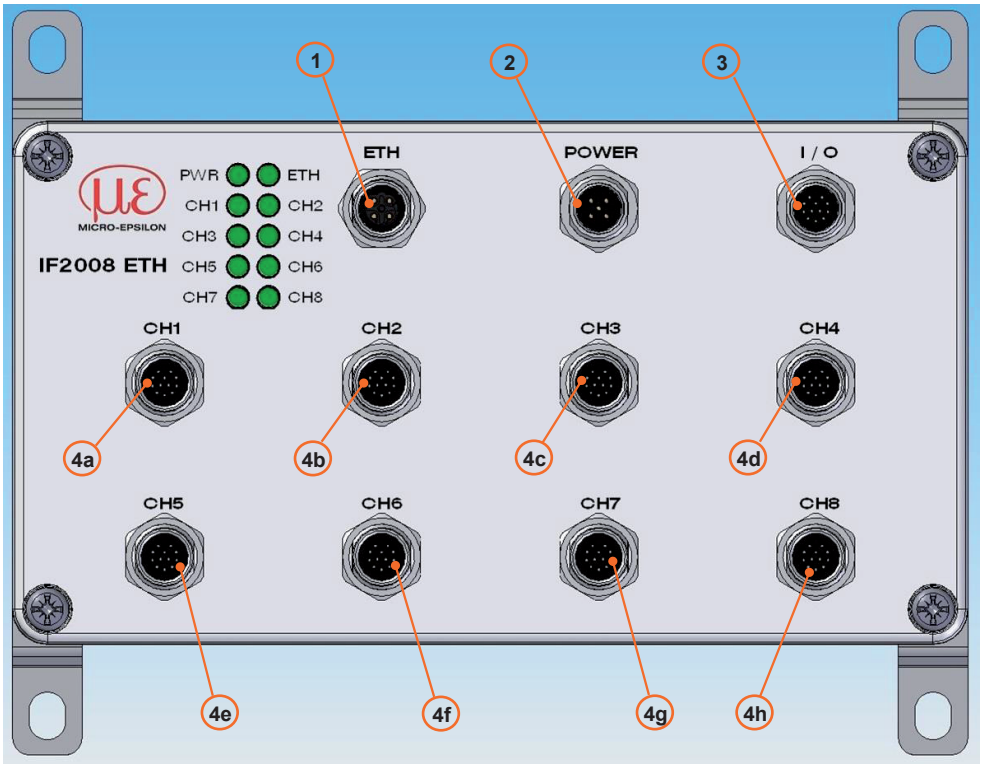


Fig. 2 Plug-in connections IF2008 ETH interface module

Connector	Description
①	Flange socket, 4-pin, type Binder 09 3732 500 04 for Ethernet connection
②	Flange connector, 5-pin, type Binder 09 3441 600 05 for power connection
③	Flange connector, 12-pin, type Binder 09 3491 600 12 for I/O connection
④a to ④h	Flange socket, 12-pin, type Binder 09 3492 600 12 for sensor/encoder connection

Fig. 3 Overview of plug-in connections

4.2 Pin Assignment

Pin assignments, see Fig. 3, are described in the following tables below, see Fig. 4 and subsequent :

Connector	Pin	Signal	Comment
①	1	Ethernet TxD+	-
	2	Ethernet RxD+	-
	3	Ethernet TxD-	-
	4	Ethernet RxD-	-

Fig. 4 Pin assignment of Ethernet interface

Connector	Pin	Function	Comment
②	1	+24 VDC [1]	Power supply for interface module and sensors
	2	+24 VDC [1]	
	3	GND	
	4	GND	
	5	Shield	

Fig. 5 Pin assignment of power connection

Connector	Pin	Function	Comment
③	1	External entrance 1	-
	2	External entrance 2	-
	3	External entrance 3	-
	4	External entrance 4	-
	5	External output 1	-
	6	External output 2	-
	7	External output 3	-
	8	External output 4	-
	9	n.c.	-
	10	n.c.	-
	11	Voltage output	LLL = +5 V, HLL = +24 V
	12	GND	-

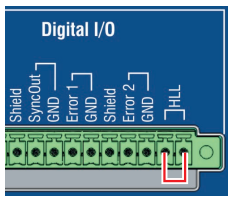


Fig. 6 Pin assignment I/O interface

Stecker	Pin	Signal IF2008ETH	Signal ILD 1420	ILD 2300	IFC 24xx
4a	1	TRG+	n.c.	TRG+	n.c.
4b	2	TRG-	n.c.	TRG-	n.c.
4c	3	TxD+	RxD+	RxD+	TxD+
4d	4	TxD-	RxD-	RxD-	TxD-
4e	5	RxD+	TxD+	TxD+	RxD+
4f	6	RxD-	TxD-	TxD-	RxD-
4g	7	+24 VDC	$+U_B$	$+U_B$ and Laser ON+	n.c.
4h	8	Laser ON-	Laser ON-	Laser ON-	n.c.
	9	Multi-function output	Multi-function output	n.c.	TRG+ (HLL) [2]
	10	ERROR input	ERROR output	n.c.	n.c.
	11	+ VDC (only for encoder)	n.c.	n.c.	n.c.
	12	GND	GND	GND	GND

Fig. 7 Pin assignment sensor interface

1) Permissible supply voltage range 11 - 30 V

2) Bridge for HLL level on the IFC 24xx controller is set.

Connector	Pin	Signal IF2008ETH	Signal Encoder
4a	1	A+	A+
	2	A-	A-
4b	3	B+	B+
	4	B-	B-
4c	5	R+	R+
	6	R-	R-
4d	7	+24 VDC [1]	n.c.
	8	Laser ON- [1]	n.c.
4e	9	Multi-function output [1]	n.c.
	10	ERROR input [1]	n.c.
4f	11	+5 VDC	+5 VDC
	12	GND	GND
4g			
4h			

Fig. 8 Pin assignment encoder interface

1) Only for sensors

4.3 LED Overview

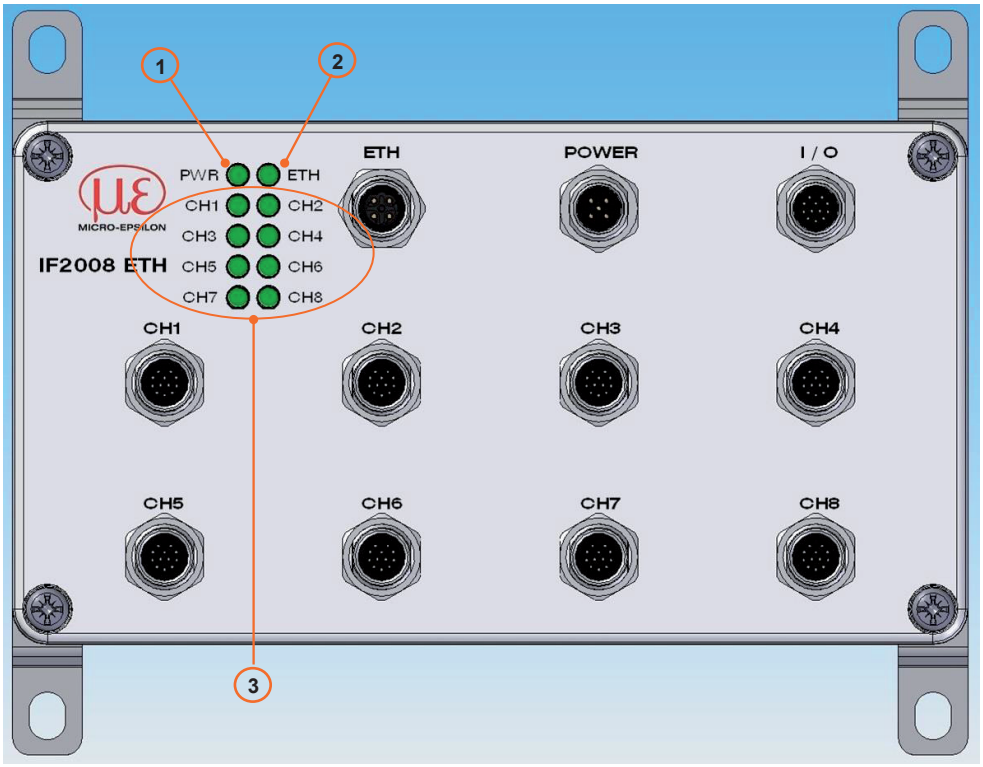


Fig. 9 Status LEDs IF2008 ETH interface module

LED	LED color	Description
①	Off	Power supply off
	Green	Interface module is ready for operation
	Orange	Interface module is in bootloader/flash mode
	Red	Initialization of the interface module
②	Off	No Ethernet connection
	Orange	Connection between PC and interface module (100 Mbps)
	Flashing	Data transmission between PC and interface module
③	Off	No sensor connected
	Green	No sensor/encoder selected
	Orange	Interface set for sensor
	Red	Interface set for sensor

Fig. 10 Description of multi-color status LED

5. Liability for Material Defects

All components of the device have been checked and tested for functionality at the factory. However, if defects occur despite our careful quality control, MICRO-EPSILON or your dealer must be notified immediately.

The liability for material defects is 12 months from delivery. Within this period, defective parts, except for wearing parts, will be repaired or replaced free of charge, if the device is returned to MICRO-EPSILON with shipping costs prepaid. Any damage that is caused by improper handling, the use of force or by repairs or modifications by third parties is not covered by the liability for material defects. Repairs are carried out exclusively by MICRO-EPSILON.

Further claims can not be made. Claims arising from the purchase contract remain unaffected. In particular, MICRO-EPSILON shall not be liable for any consequential, special, indirect or incidental damage. In the interest of further development, MICRO-EPSILON reserves the right to make design changes without notification.

For translations into other languages, the German version shall prevail.

6. Service, Repair

If the interface module is defective please send us the affected parts for repair or exchange.

If the cause of a fault cannot be clearly identified, please send the entire measuring system to:

MICRO-EPSILON MESSTECHNIK
GmbH & Co. KG
Koenigbacher Str. 15
94496 Ortenburg / Germany

Tel. +49 (0) 8542 / 168-0
Fax +49 (0) 8542 / 168-90
info@micro-epsilon.com
www.micro-epsilon.com

7. Decommissioning, Disposal

➪ Remove all cables on the interface module.

Incorrect disposal may cause harm to the environment.

➪ Dispose of the device, its components and accessories, as well as the packaging materials in compliance with the applicable country-specific waste treatment and disposal regulations of the region of use.

Appendix

A 1 Accessories

Name	Description	Article Number
PC2008-5/M12 Power supply cable, 5m	M12 on one side, socket, one side open ends, 5-pin, A-coded, suitable for use with robots and drag chains, 5 m long	29011310
SCD2520-3 Digital output cable, 3 m long	Digital output cable, 3 m long to connect an Ethernet/EtherCAT interface, angled 4-pin M12 plug on one side, RJ45 plug on other side, 3 m long	2901925
PCE1420-2/M12 Sensor cable extension, 2 m	M12 on both sides, plug socket, 12-pin, A-coded, assignment is identical to ILD1420 standard cable, suitable for use with robots and drag chains, 2 m long	29011149
SC2471-3/IF2008ETH Connector cable, 3 m	Connection cable to connect a confocal IFC 24xx controller, 3 m long	29011145
PCE2300-3/M12 Extension cable, 3 m	Power supply and output cable to connect an ILD2300 on the IF2008/ETH, 3 m long	29011279

A 2 ASCII Communication with Sensor

Command port 23 protocol (Telnet)

A 2.1 Commands Overview

Group	Chapter	Command	Short info
General			
	Information		
	Chap. A 2.2.1.1	GETINFO	IF2008/ETH information
	Chap. A 2.2.1.2	GETINFOn	Sensor information
	Chap. A 2.2.1.3	PRINT	Parameter overview
	Interfaces		
	Chap. A 2.2.2.1	IPCONFIG	Ethernet settings
	Chap. A 2.2.2.2	MEASTRANSFER	Setting measurement server
	Chap. A 2.2.2.3	MEASCNT_ETH	Size of TCP / IP packets
	Chap. A 2.2.2.4	LANGUAGE	Language webinterface
	Chap. A 2.2.2.5	CHANNELMODE	Operating mode
	Timer		
	Chap. A 2.2.3.1	TIMERFREQUENCYn	Timer frequency
	Chap. A 2.2.3.2	TIMERPULSEWIDTH	Timer pulse width
	Parameter management		
	Chap. A 2.2.4.1	STORE	Save parameters
	Chap. A 2.2.4.2	READ	Read parameters
	Chap. A 2.2.4.3	SETDEFAULT	Factory settings
	Chap. A 2.2.4.4	RESET	Restarting IF2008/ETH
Sensor			
	Settings		
	Chap. A 2.3.1.1	BAUDRATE	Sensor channel baudrate
	Chap. A 2.3.1.2	LASERPOW	Sensor laser outputs
	Chap. A 2.3.1.3	TRIGGEROUTPUT	Trigger outputs
	Functions		
	Chap. A 2.3.2.1	SENSORERROR	Sensor error inputs
	Chap. A 2.3.2.2	TUNNELn ``...``	Tunneling sensor commands
	Chap. A 2.3.2.3	TUNNELn ...	Tunneling sensor commands
Encoder			
	Settings		
	Chap. A 2.4.1.1	ENCINTERPOL	Encoder interpolation type
	Chap. A 2.4.1.2	ENCREF	Encoder behavior at reference
	Chap. A 2.4.1.3	ENCVALUE	Encoder default value
	Chap. A 2.4.1.4	ENCDIR	Encoder counting direction
	Chap. A 2.4.1.5	ENCLATCHSRC	Encoder detection source
	Functions		
	Chap. A 2.4.2.1	ENCSET	Set encoder value
	Chap. A 2.4.2.2	ENCRESET	Reset reference marks
	Chap. A 2.4.2.3	ENCCLEAR	Rest encoder
	Chap. A 2.4.2.4	GETENVALUE	Query encoder value
	Chap. A 2.4.2.5	GETENCREF	Query reference counter
Digital I/O			
	General		
	Chap. A 2.5.1.1	EXTLEVEL	Digital logic
	Schalteingänge		
	Chap. A 2.5.2.1	EXTINLATCHSRC	Digital inputs detection source
	Chap. A 2.5.2.2	GETEXTINPUT	Query digital inputs
	Chap. A 2.5.2.3	EXTINPUTMODE1	Programming digital input 1
	Chap. A 2.5.2.4	EXTINPUTMODE2	Programming digital input 2
	Chap. A 2.5.2.5	EXTINPUTMODE3	Programming digital input 3
	Schaltausgänge		
	Chap. A 2.5.3.1	EXTOUTSRC	Programming digital outputs

A 2.2 General Commands

A 2.2.1 Information

A 2.2.1.1 IF2008/ETH Information

```
GETINFO
```

Controller data are queried. Output as per example below:

```
->GETINFO
Name:              IF2008ETH
Serial:            17000000
Option:            000
Article:           2213030
MAC-Address:       00-0C-12-02-04-3F
FPGA-Version:      16
MAC-Address:       7480
Boot-Version:      0.1.01
Version:           0.0.08
->
```

A 2.2.1.2 Sensor Information

```
GETINFOn
```

n = 0 ... 8

Outputs the corresponding sensor's information.

n = 0: Information for all sensors

A 2.2.1.3 Parameter Overview

```
PRINT [ALL]
```

- No parameter: This command outputs a list of all setting parameters and its values.
- ALL: This command outputs a list of all setting parameters and their values, as well as additional information, such as `GETINFO`.

A 2.2.2 Interfaces

A 2.2.2.1 Ethernet Settings

```
IPCONFIG DHCP|STATIC [<IPAdresse> [<Netmask> [<Gateway>]]]
```

Setting of the Ethernet interface.

- DHCP: If no DHCP server is available, a link-local address is searched for after approx. 30 seconds.
- STATIC: Sets an IP address, the net mask and the gateway in IPv4 format as xxx.xxx.xxx.xxx

If the IP address, net mask and/or gateway are not stated, their values remain unchanged.

A 2.2.2.2 Setting Measurement Server

```
MEASTRANSFER SERVER/TCP [<PORT>]
```

Measured value output currently only on TCP server.

- The port is freely selectable between 1024 and 65535.

A 2.2.2.3 Size of TCP / IP Packets

```
MEASCNT_ETH <TupelCnt>
```

- Specifies the number of data tuples that are transmitted in one Ethernet packet. A data tuple consists of an address byte and a data byte. The format is described in Appendix, see A 2.6.
- 0: The number of data tuples is determined automatically to allow an Ethernet packet to be sent every 10 ms on average.
- 1 ... 716: Number of data tuples in an Ethernet packet. If the packets cannot be sent quickly enough, this value is exceeded.

A 2.2.2.4 Language Webinterface

```
LANGUAGE BROWSER|ENGLISH|GERMAN
```

Language of the displayed web pages

- BROWSER: The display language is determined by the web browser.

A 2.2.2.5 Operating Mode

```
CHANNELMODEn NONE|SENSOR|ENCODER
```

n= 1..8 for the sensor /encoder channels 1 to 8.

Channels can be switched between sensor or encoder mode.

- NONE: Channel is deactivated.
- SENSOR: The channel is configured to record sensor data.
- ENCODER: The channel is configured for encoder operation.

A 2.2.3 Timer

A 2.2.3.1 Timer Frequency

```
TIMERFREQUENCYn <Frequency>
```

n = 1 ... 3 for the timers 1 to 3

Defining the frequency of the internal timer

The frequency can be freely adjusted from 0.1 Hz to 12 MHz (in Hz with three decimal places). The IF2008/ETH internally selects the next possible frequency which is supported.

A 2.2.3.2 Timer Pulse Width

```
TIMERPULSEWIDTHn <Pulsewidth>
```

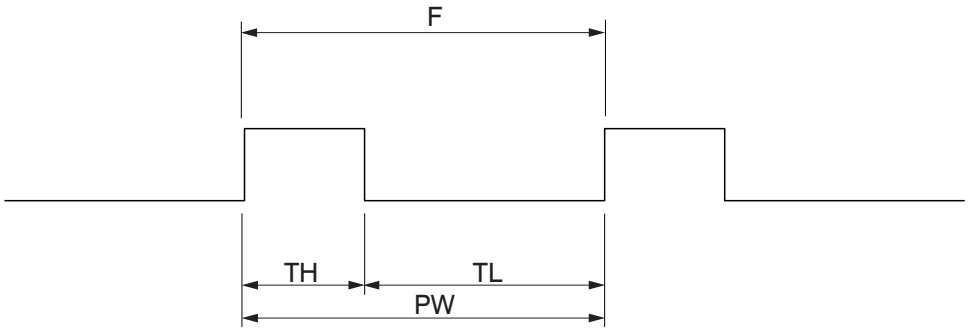
n = 1 ... 3 for the timer 1 to 3

Pulse width modulation of a timer cycle.

Determines the pulse width modulation of the timer signal; that is, the ratio of high to low portions of the timer signal in percent.

Pulse width modulation can be set between 0 (0 %) and 1 (100 %). Three decimal points are permitted. Internally, IF2008/ETH selects the next possible supported pulse width modulation.

A pulse width modulation of 0.5 means that the high and low portions of the timer signal have the same lengths. A pulse width modulation greater than 0.5 means that the high portion of the timer signal is longer than the low portion. A pulse width modulation smaller than 0.5 means that the high portion of the timer signal is shorter than the low portion.



F = Timer frequency
TH = Timer signal high
TL = Timer signal low
Timer pulsewidth = PW / (TH + TL)

Fig. 11 Timer frequency and timer pulse width

A 2.2.4 Parameter Management

A 2.2.4.1 Save Parameters

```
STORE 1|2|3|4|5|6|7|8
```

Save the current parameters under the specified number in the flash memory of IF2008/ETH.

A 2.2.4.2 Read Parameters

```
READ ALL|DEVICE|MEAS 1|2|3|4|5|6|7|8
```

Read the parameters under the specified number from the flash memory of IF2008/ETH.

The volume of data to be loaded must also be specified:

- ALL: All parameters are loaded.
- DEVICE: Only the basic device settings are loaded (interface parameters).
- MEAS: Only the measurement settings are loaded (all properties for the measurement).

A 2.2.4.3 Factory Settings

```
SETDEFAULT [ALL] [NODEVICE]
```

Reset to factory settings

- ALL: All setups are reset to factory settings. If ALL is not specified, only the current setup is reset.
- NODEVICE: Only the settings for measurements are reset, the settings for interfaces are maintained.

A 2.2.4.4 Restarting IF2008/ETH

```
RESET
```

Restarts the IF2008/ETH.

A 2.3 Sensor

A 2.3.1 Settings

A 2.3.1.1 Sensor Channel Baudrate

```
BAUDRATEn <Baudrate>
```

n = 1 ... 8 for the sensor channels 1 to 8.

Setting the interface baud rate on the IF2008/ETH for the respective sensor channel.

The baud rate can be freely adjusted from 9600 bauds to 8 Mbaud. The IF2008/ETH internally selects the next possible baud rate which is supported.

A 2.3.1.2 Sensor Laser Outputs

```
LASERPOWn OFF|ON
```

n = 1 ... 8 for the sensor channels 1 to 8.

Switches the connection for laser activation (pin 8)

- OFF: Laser is off
- ON: Laser is on

A 2.3.1.3 Trigger Outputs

```
TRIGGEROUTPUTn LOW|HIGH|TIMER1|TIMER2|TIMER3|INPUT1|INPUT2|INPUT
3|INPUT4
```

n = 1 ... 8 for the sensor channels 1 to 8.

Selects the source for the trigger outputs on the sensor channels (pins 1+2 or pin 9).

- LOW, HIGH: Output has this fixed state
- TIMER1 ... 3: A timer switches the output
- INPUT1 ... 4: Output has the state of a digital input

A 2.3.2 Functions

A 2.3.2.1 Sensor Error Inputs

```
SENSORERROR
```

Returns the bit-coded state of the error line (pin 10) of all sensor channels (bit 0 = error state of sensor 1, bit 1 = error state of sensor 2, ...) as a decimal value.

The return value can be between 0 (no sensor reports an error) and 255 (all sensors report an error).

A 2.3.2.2 Tunneling Sensor Commands

```
TUNNELn “...“
```

n = 1 ... 8 for the sensor channels 1 to 8.

Returns the command in quotation marks to the respective sensor channel. The reply is returned from the data socket.

A quotation mark in the command must be quoted with a backlash, i.e. “ -> \“. The same applies for a backlash itself, i.e. \ -> \\.

Carriage return can be quoted with \r and line feed with \n. Arbitrary binary sequences are entered with \xhh (hh is a hexadecimal code).

i Sensors with ASCII protocol (e.g. ILD2300) must contain the final \r\n within the quotation marks.

A 2.3.2.3 Tunneling Sensor Commands (ASCII Version)

```
TUNNELn ...
```

n = 1 ... 8 for the sensor channel 1 to 8.

Pure ASCII variant of tunnel command for easy entry via e.g. telnet.

The final carriage return of the tunnel command is also sent to the sensor so it recognizes the end of the command sequence.

A 2.4 Encoder

A 2.4.1 Settings

A 2.4.1.1 Encoder Interpolation Type

```
ENCINTERPOLn COUNTER|1|2|4
```

n = 1 ... 8 for the encoder channnels 1 to 8.

Setting the interpolation depth of each encoder input.

- COUNTER: Normal counter mode
- 1, 2, 4: Interpolation stage (Single/double/quadruble evaluation)

A 2.4.1.2 Encoder Behavior at Reference

```
ENCREFn NONE|ONE|EVER|LIMIT
```

n = 1 ... 8 for the encoder channels 1 to 8.

Setting the effect of encoder reference track.

- NONE: Reference mark of encoder has no effect.
- ONE: Setting once (the encoder value (see ENCVALUEn) is taken over when the reference mark position is reached for the first time).
- EVER: Setting at all mark positions (the encoder value is taken over every time the reference marker position is reached).
- LIMIT: The encoder is limited between 0 and encoder value (see ENCVALUEn). When exceeding the threshold, the value is set to the opposite value (forward encoder value -> 0, backward 0 -> encoder value)

A 2.4.1.3 Encoder Default Value

```
ENCVALUEn <Encoder value>
```

n = 1 ... 8 for the encoder channels 1 to 8.

Indicates the value to which the corresponding encoder is to be set when reaching a reference mark position (or via software).

The encoder value can be set between 0 and 4294967295 (UINT_MAX).

A 2.4.1.4 Encoder Counting Direction

```
ENCDIRn NORMAL|REVERSE
```

- ENCDIR NORMAL: A is counting direction, B is counter clock
- ENCDIR REVERSE: reverse, C is always used to reset the counter

In the `NORMAL` setting, encoder track A determines the counting direction and encoder track B the counter clock; in the `REVERSE` setting, the exact opposite is true. Encoder track C is always used to reset the counter.

n = 1 ... 8 for the encoder channels 1 to 8.

Counting direction of encoder.

A 2.4.1.5 Encoder Detection Source

```
ENCLATCHSRCn NONE|TIMER1|TIMER2|TIMER3|SENSOR1|SENSOR2|SENSOR3|S
ENSOR4|SENSOR5|SENSOR6|SENSOR7|SENSOR8|INPUT1|INPUT2|INPUT3|INPU
T4|SECONDREF|ANYREF
```

n = 1 ... 8 for the encoder channels 1 to 8.

Selects the source with which the encoder value is written in the IF2008/ETH FIFO (for continuous recording).

- NONE: No automatic encoder record.
- TIMER1 ... 3: Encoder is recorded using a timer.
- SENSOR1 ... 8: Synchronous encoder record along with data frames of a sensor.
- INPUT1 ... 4: Encoder record with rising edge of a digital input.
- SECONDREF: Encoder record when second reference mark is reached.
- ANYREF: Encoder record with each reference mark.

A 2.4.2 Functions

A 2.4.2.1 Set Encoder Value

```
ENCSET 1|2|3|4|5|6|7|8
```

Setting the encoder preset values (see ENCVALUEn) in the indicated encoder.

A 2.4.2.2 Reset Reference Marks

```
ENCRESET 1|2|3|4|5|6|7|8
```

Reset the Detection of the First Mark Position (see ENCREFn).

A 2.4.2.3 Reset Encoder

```
ENCCLEAR 1|2|3|4|5|6|7|8
```

Resetting the encoder value to 0 in the indicated encoder.

A 2.4.2.4 Query Encoder Value

```
GETENCVALUEn
```

n = 1 ... 8 for the encoder channels 1 to 8.

Asynchronous read-out of current encoder value. The return value can be between 0 and 4294967295 (UINT_MAX).

A 2.4.2.5 Query Reference Counter

```
GETENCREFn
```

n = 1 ... 8 for the encoder channels 1 to 8.

Request reference counter state.

- NONE: Reference mark not crossed since the last reset.
- FIRST: Reference mark crossed once.
- SECOND: Reference mark crossed several times.

A 2.5 Digital I/O

A 2.5.1 General

A 2.5.1.1 Digital Logic

```
EXTLEVEL LLL|HLL
```

Defines the logic level of the digital inputs/outputs

- LLL: Low level logic (Low 0.2 - 0.8 V High 4.5 - 5 V)
- HLL: High level logic (Low 0.2 - 0.8 V High 23.5 - 24 V)

A 2.5.2 Switching Inputs

A 2.5.2.1 Digital Inputs Detection Source

```
EXTINLATCHSRC NONE|TIMER1|TIMER2|TIMER3|SENSOR1|SENSOR2|SEN-
SOR3|SENSOR4
```

Selects the source with which the values of the digital inputs are written in the IF2008/ ETH FIFO (for continuous record).

- NONE: Digital inputs are not automatically recorded.
- TIMER1 ... 3: Digital inputs are recorded using a timer.
- SENSOR1 ... 4: Synchronous record of digital inputs along with data frames of a sensor.

A 2.5.2.2 Query Digital Inputs

```
GETEXTINPUT
```

Asynchronous, bit-coded, decimal read-out of current state of digital inputs (bit 0 = input 1, bit 1 = input 2, ...) as a decimal value. The return value can be between 0 and 15.

A 2.5.2.3 Programming Digital Input 1

```
EXTINPUTMODE1 NONE|LASERPOW
```

Function of digital input 1

- NONE: No special function
- LASERPOW: Switches the cable for laser activation in all channels (is AND-linked with LASERPOWn, i.e. only when both signals are on, laser is on.)

A 2.5.2.4 Programming Digital Input 2

```
EXTINPUTMODE2 NONE|FIFOGATE
```

Function of digital input 2

- NONE: No special function
- FIFOGATE: Locks the IF2008/ETH FIFO with high signal for the sensor/encoder channels 1 - 4

A 2.5.2.5 Programming Digital Input 3

```
EXTINPUTMODE3 NONE|FIFOGATE
```

Function of digital input 3

- NONE: No special function
- FIFOGATE: Locks the IF2008/ETH FIFO with high signal for the sensor/encoder channels 5 - 8

A 2.5.3 Switching Outputs

A 2.5.3.1 Programming Digital Outputs

```
EXTOUTSRCn LOW|HIGH|TIMER1|TIMER2|TIMER3
```

n = 1 ... 4 for the digital outputs 1 to 4

Selects the source for the digital outputs

- LOW, HIGH: Output has this fixed state
- TIMER1 ... 3: Output is switched using the corresponding timer.

A 2.6 Measurement Data Transmission to a Measurement Value Server, Measurement Value Block

Each data packet includes a header (28 bytes) and the following data.

Preamble (32 bits)	
Article number (32 bits)	
Serial number (32 bits)	
Flags 1 (32 bits)	
Flags 2 (32 bits)	
Number of tuples (16 bits)	Bytes per tuple (16 bits)
Counter (32 bits)	

Fig. 12 Measurement value block header

Header registration	Description
Preamble (32 bit)	MEAS
Article number (32 bit)	2213030
Serial number (32 bit)	32 bits
Flags 1 (32 bit)	Bit 0 ... 15: Respectively two bits describe a data channel. 00 = off, 01 = Encoder, 10 = Sensor, 11 = Reserved (CHANNELMODEn), Bit 16: Indicates if digital values are active. (EXTINLATCHSRC) Bit 17 ... 30: reserved, always 0 Bit 31: Indicates whether an overflow has occurred in the FIFO of the IF2008/ETH (data loss)
Flags 2 (32 bit)	Reserved, permanent 0
Number of tuples (16 Bit)	Number of tuples in packet
Bytes per tuple (16 Bit)	2 (each tuple consists of 2 bytes)
Counter (32 Bit)	Global, continuous tuple counter for all packets. The first packet has the value 0, so it will only be incremented after output.

Fig. 13 Inputs in the measurement value block header

Data:

Each sensor byte is equipped with another address byte and stored as tuple (first address and then data byte).

Address byte (8 bits):	Bits 0 ... 2:	Byte counter (0 - 7), starts from 0 after every break and stops at 7 with longer data frames from a sensor.
	Bits 3 ... 5:	Sensor/encoder channel (0 - 7) corresponds to the channel 1 to 8
	Bits 6 ... 7:	Data source: 00 = sensor, 01 = encoder, 10 = DigitalIn, 11 = reserved
Data byte (8 bits):		As received by the sensor

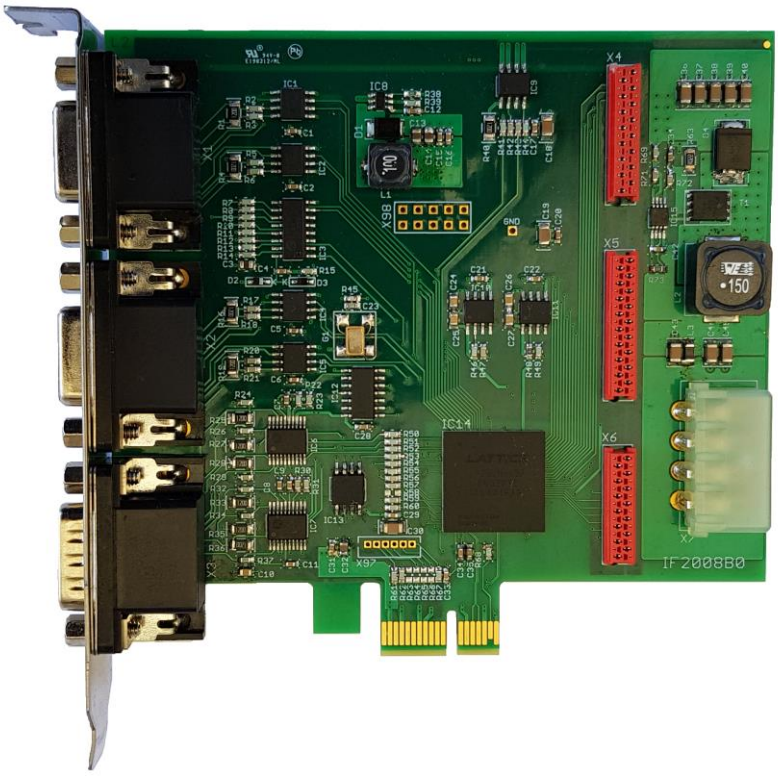
Encoder transmission is always with 32 bits, i.e. four successive tuples.

DigitalIn is transmitted with 4 bits (upper four bits are 0), i.e. one tuple.

MICRO-EPSILON

Description

IF2008/PCIe PCI Basis Board
IF2008E Expansion Board



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1 Technical Data

1.1 IF2008/PCIe Basis Board

Mechanics and environment

- Dimensions (PCB) approx. 110 x 105 mm, width: 1 slot
- Max. permitted ambient temperature +40 °C
- 2x D-SUB female connectors HD 15-pin for sensor connections
- 1x D-SUB male connector HD 15-pin for encoder signals
- 1x Tyco/AMP Commercial MATE-N-LOK connector (IDE hard-drive connector) for supply of DC/DC converter
- 3x Tyco/AMP MicroMatch female connectors for connection to IF2008E

PCI-Express bus

- PCI-Express x1 interface
- Target interface (slave) according to specification Rev 1.0)
- Current consumption at +3.3 V approx. 0.5 A, without sensors and encoders
- Power supply of encoders with +5 V from the PCI power
- Power supply of the sensors with +24 V from the PC power supply

Sensor interface (X1 / X2)

- 4x RS422 drivers (2x TxD and 2x trigger out) and 2x RS422 receivers per connector (input/output frequency max. 5 MHz)
- Power supply of sensors with 24 V

Encoder interface (X3)

- Interface for two encoders with 1Vss, RS422 (difference) or TTL (single-ended) signals
- Power supply of the encoders with +5 V from PCI power supply without galvanic isolation (current consumption dependent on the connected encoders)
- Interpolation programmable from 1 to 64 times for encoders with 1Vss signals (input frequency max. = [3.2 MHz / interpolation] ≤ 800 kHz)
- Evaluation programmable from 1 to 4 times for encoders with:
  Rs422-/Difference signals (input frequency max. 800 kHz)
  TTL-/Single-ended signals (input frequency max. 400 kHz)

1.2 IF2008E Expansion Board

Mechanics and environment

- Dimensions (PCB) approx. 71 x 102 mm, width: 1 slot
- Max. permitted ambient temperature +40 °C
- 1x D-SUB female connector HD 15-pin for sensor connections
- 1x D-SUB female connector 9-pin for IO interface
- 1x D-SUB male connector 9-pin for analog inputs
- 3x MicroMatch female connectors for connection to IF2008/PCIe

Sensor interface (X1)

- Identical to IF2008/PCIe (X1)

IO interface (X2)

- 4x Optocoupler inputs, input current max. 5 mA, input frequency max. 1 MHz
- 4x Optocoupler outputs, output current max. 20 mA, output frequency max. 1 MHz

Analog interface (X3)

- 2x ADC channels
- Input voltage range 0-5 V, 0-10 V, ± 5 V, ± 10 V, separately adjustable for each channel via DIP switch
- Resolution 16 bits
- Offset error max. ± 3 mV
- Gain error max. ± 5 mV
- Conversion rate max. 150 kHz per channel

2 Hardware

2.1 View of IF2008/PCIe Basis Board

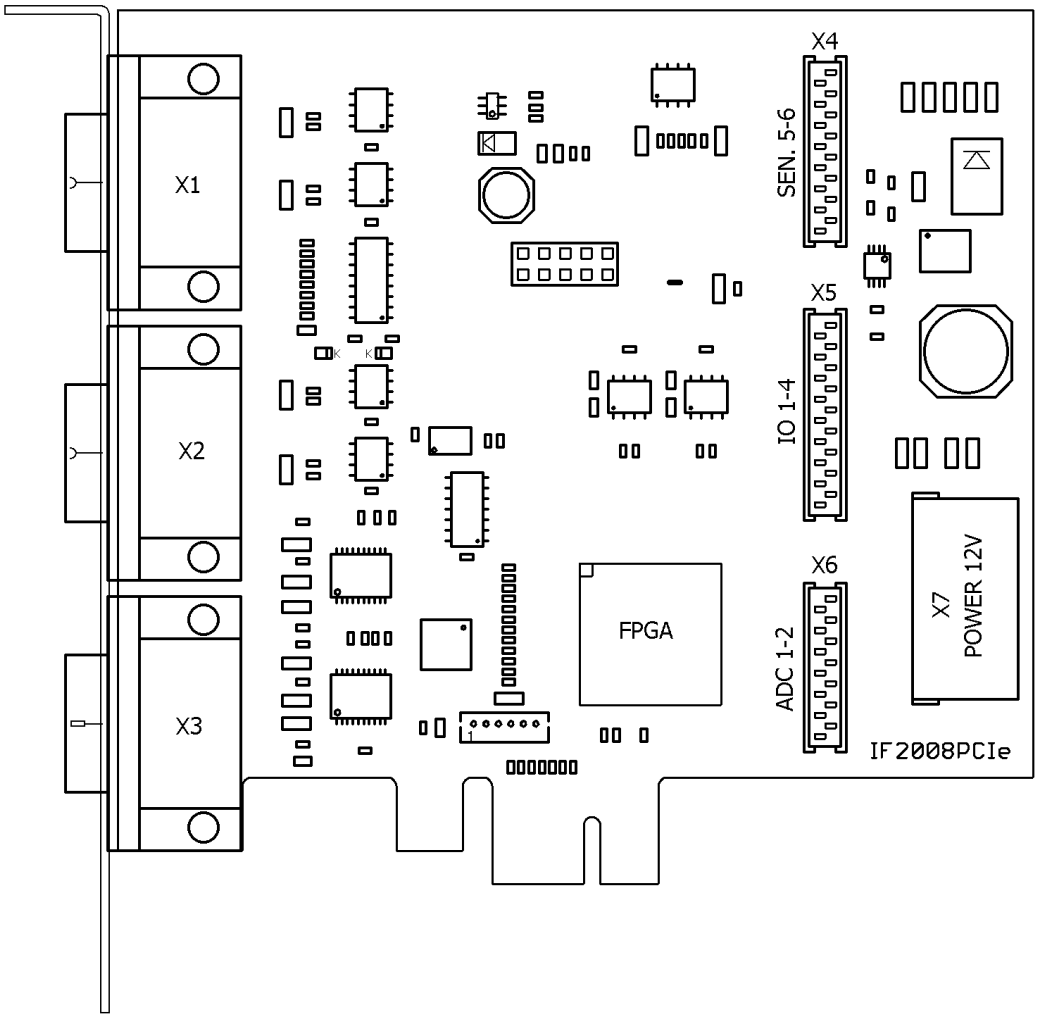


Figure 1: View of board IF2008/PCIe Basis Board

- X1 = Sensor connection 1 and 2
- X2 = Sensor connection 3 and 4
- X3 = Encoder connection 1 and 2
- X4 ... X6 = Connector for IF2008E connection
- X7 = Connection 12 V power

2.2 View of IF2008E Expansion Board

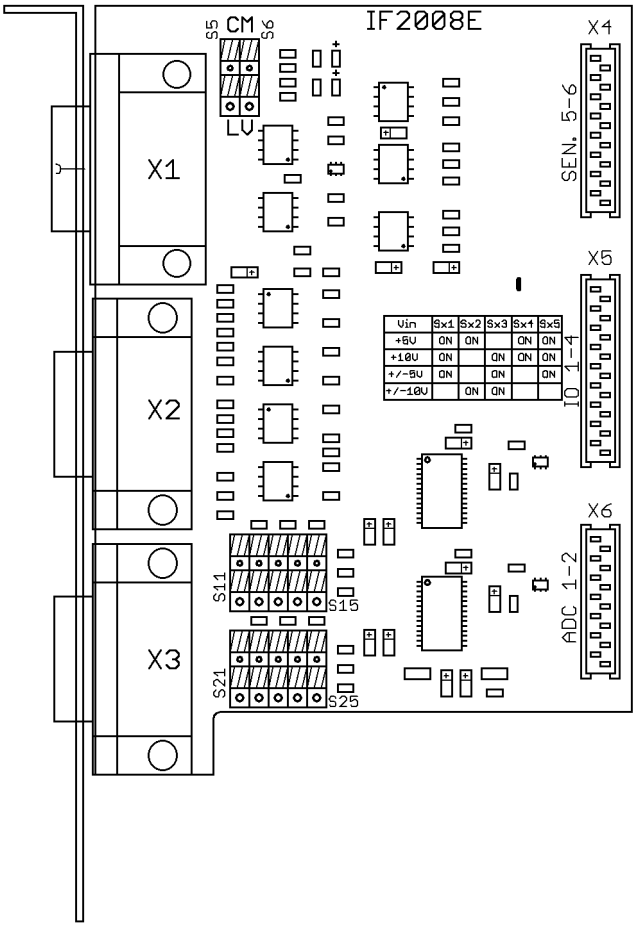


Figure2: View of board IF2008E expansion board

- X1 = Sensor connection 5 and 6
- X2 = Connection for IO signals
- X3 = Connection for A/D converter
- X4 ... X6 = Connection for IF2008/PCIe connection
- S5 and S6 = Switch for positive trigger level
- S11 ... S15 = Switch for ADC level 1
- S21 ... S25 = Switch for ADC level 2

3 Pin Assignment and Jumper Settings

3.1 Sensor Interface (IF2008/PCIe X1 and X2, IF2008E X1)

Pin	Signal
1	Sensor 1 TxD-
2	Sensor 1 TxD+
3	Sensor 1 RxD-
4	Sensor 1 RxD+
5	GND
6	Sensor 1 TRG+
7	Sensor 1 TRG-
8	Sensor 2 TRG+
9	Sensor 2 TRG-
10	Power supply +24V
11	Sensor 2 TxD-
12	Sensor 2 TxD+
13	Sensor 2 RxD-
14	Sensor 2 RxD+
15	GND

Table 1: Pin assignment for sensor interface

3.2 Encoder Interface (IF2008/PCIe X3)

Pin	Function
1	Encoder 1 Track A+
2	Encoder 1 Track A-
3	Encoder 2 Track A+
4	Encoder 2 Track A-
5	VCC (+5 V)
6	Encoder 1 Track B+
7	Encoder 1 Track B-
8	Encoder 2 Track B+
9	Encoder 2 Track B-
10	GND
11	Encoder 1 Track R+
12	Encoder 1 Track R-
13	Encoder 2 Track R+
14	Encoder 2 Track R-
15	GND

Table 2: Pin assignment for encoder interface

Attention: The pin assignment is **not** compatible with IF2004B!

3.3 Sensor Power (IF2008/PCIe X7)

Pin	Function
1	+12V
2	GND
3	GND
4	n.c.

Table 3: Pin assignment of sensor power

3.4 IO Interface (IF2008E X2)

Pin	Function
1	OUT1
2	OUT2
3	OUT3
4	OUT4
5	GND
6	IN1
7	IN2
8	IN3
9	IN4

Table 4: Pin assignment IO interface

3.5 Analog Interface (IF2008E X3)

Pin	Function
1	Input signal 1
2	Analog GND
3	Input signal 2
4	Analog GND
5	n.c.
6	n.c.
7	n.c.
8	n.c.
9	n.c.

Table 5: Pin assignment analog interface

3.6 Jumper/Switch Setting for Trigger Level

By means of the switches S5 and S6 (IF2008E) the positive trigger level for the sensor channels 5 and 6 (IF2008A) can be selected. The negative output always has LVDS level.

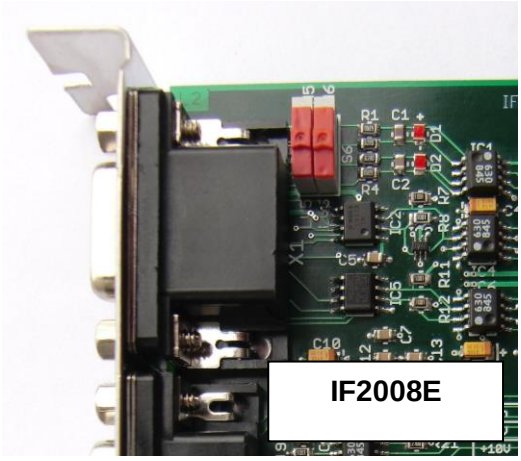


Figure 3: Switch settings trigger level

Switch	Setting	Trigger output +
S5 to S6	LVn	LVDS-Level for sensor n TRG+
	CMn	3.3 V CMOS level for sensor n TRG+

Table 6: Switch settings trigger level

3.7 Switch Setting for ADC Level

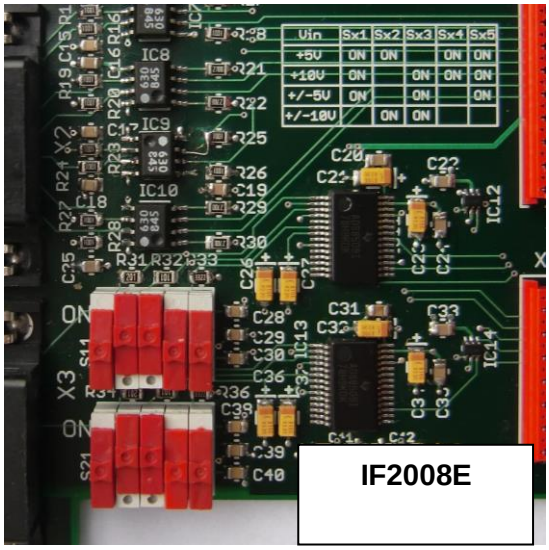


Figure 4: Switch settings ADC level
(±10 V are set in the figure)

VIN	Sx1	Sx2	Sx3	Sx4	Sx5
0-5 V	ON	ON		ON	ON
0-10 V	ON		ON	ON	ON
±5 V	ON		ON		ON
±10 V		ON	ON		

Table 7: Switch settings ADC level

4 Address Assignment

4.1 PCI Interface

Interface: PCI-Express x1 interface
Access: Memory space 40 Hex addresses
Base address: Automatically assigned by operating system

Header configuration

Addr.	Byte 3	Byte 2	Byte 1	Byte 0	Value (Hex)
00h	Device ID		Vendor ID		1910 1204
18h	Base Address Local Memory Space				xxxx xxxx
2C	Subsystem ID		Subsystem Vendor ID		2008 1204

Table 8: Header configuration

4.2 Local Address Assignment

Base addr. +	Write access	Read access
00h	Transmit register	FIFO data
02h	Set- / Reset- / Latch register	FIFO volume
04h	FIFO enable register	FIFO enable register
06h	Interrupt enable register	Interrupt status register
08h	Sensor 1 baud rate	Reserved
0Ah	Sensor 2 baud rate	Reserved
0Ch	Sensor 3 baud rate	Reserved
0Eh	Sensor 4 baud rate	Reserved
10h	Sensor 5 baud rate	Reserved
12h	Sensor 6 baud rate	Reserved
14h	Counter control register 1	Counter control register 1
16h	Counter control register 2	Counter control register 2
18h	Counter 1 preload LSW	Counter 1 LSW
1Ah	Counter 1 preload MSW	Counter value 1 MSW
1Ch	Counter 2 preload LSW	Counter 2 LSW
1Eh	Counter 2 preload MSW	Counter value 2 MSW
20h	Timer 1 frequency	ADC 1
22h	Timer 1 pulse width	ADC 2
24h	Timer 2 frequency	Status, FPGA-/ hardware version
26h	Timer 2 pulse width	Input and status power switch
28h	Timer 3 frequency	Reserved
2Ah	Timer 3 pulse width	Reserved
2Ch	Timer clock splitter	Timer clock splitter
2Eh	Output register	Output register
30h	Mode opto- and TxD outputs	Mode opto- and TxD outputs
32h	Trigger Outputs Mode	Mode trigger outputs, latch source and sensor power switch
34h	ADC control register	ADC control register
36h	Parity enable register	Parity error

Table 9: Local address assignment

5 Register Description

5.1 Transmit Register

Base addr. + 00h (write access)

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
			S6	S5	S4	S3	S2	S1	D7	D6	D5	D4	D3	D2	D1	D0
	Selection sensor channel								Data bits							

Table 10: Transmit register

Bits 0 to 7 Include the data for the transmit register
Bits 8 to 15 Select the sensor channel

Bit 8 = 1 ➔ Data are output on the sensor channel S1
Bit 9 = 1 ➔ Data are output on the sensor channel S2
etc.
Bit 13 = 1 ➔ Data are output on the sensor channel S6
Bits 14..15 ➔ free

Immediately on the write access to the address “0”, the data with the bit 8 to 13 selected sensor channel are transmitted. The baud rate for the transmit register is automatically adapted to the selected sensor channel. In case that the data output is effected on more channels, the baud rate of the best channel is used.

5.2 FIFO Data

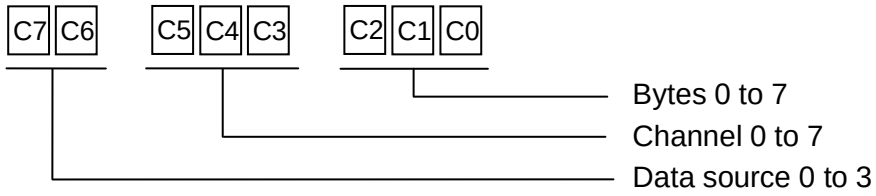
Base addr. + 00h (read access)

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	C7	C6	C5	C4	C3	C2	C1	C0	D7	D6	D5	D4	D3	D2	D1	D0
	Code bits								Data bits							

Table 11: FIFO data memory

Bits 0 to 7 Include the data buffered
Bits 8 to 15 Mark the data code

Code bits



C7	C6	Data source
0	0	Sensor
0	1	Encoder
1	0	Switching input (IN 1..4 → channel 0, RxD 1..6 → channel 1)
1	1	ADC

Table 12: FIFO data memory – data sources

5.3 Set-/ Reset-/ Latch Register

Base addr. + 02h (write access)

Bit	Function
0	Delete counter 1
1	Load counter 1
2	Latch counter 1
3	Reference counter 1
4	Delete counter 2
5	Load counter 2
6	Latch counter 2
7	Reference counter 2
8	Start ADC1 conversion
9	Start ADC2 conversion
10	Delete FIFO
11 – 15	Reserved

Table 13: Set- / Reset- / Latch register

Please note:

- By means of the bits 0 to 2 and 4 to 6, the counters can be either deleted or loaded independently of the counter control register by the software, (addr. 14h and addr. 16h). Furthermore, the counter reading can be transferred into the latch register.
- If a counter latch or load function, which should only operate in connection with a reference marker signal is settled by the counter control register (addr. 14h and addr. 16h); this is subject to approval by setting bit 3 or bit 7. On setting bit 3 or bit 7 the status bits 0 and 1 or 2 and 3 are reset.
- All bits only need to be set, resetting them is not necessary.
- After power interruption, all bits are set to “0”.

5.4 FIFO Volume

Base addr. + 02h (read access)

Bit	Function
0 to 14	FIFO data volume (0 to 32767)
15	permanently 0

Table 14: FIFO volume

The dataset is transferred automatically into the FIFO data memory on receipt. By means of a report of the FIFO volume the FIFO data amount can be calculated. The order and speed regarding buffering the data received, is similar to the data stream of the receiving register. In case that the FIFO is not readout quickly enough, it offers the latest 32768 data sets.

5.5 FIFO Enable Register

Base addr. + 04h (read and write access)

Bit	Function
0	0 = FIFO for sensor channel 1 disabled 1 = FIFO for sensor channel 1 enabled
1	0 = FIFO for sensor channel 2 disabled 1 = FIFO for sensor channel 2 enabled
2	0 = FIFO for sensor channel 3 disabled 1 = FIFO for sensor channel 3 enabled
3	0 = FIFO for sensor channel 4 disabled 1 = FIFO for sensor channel 4 enabled
4	0 = FIFO for sensor channel 5 disabled 1 = FIFO for sensor channel 5 enabled
5	0 = FIFO for sensor channel 6 disabled 1 = FIFO for sensor channel 6 enabled
6	0 = FIFO for encoder channel 1 disabled 1 = FIFO for encoder channel 1 enabled
7	0 = FIFO for encoder channel 2 disabled 1 = FIFO for encoder channel 2 enabled
8	0 = FIFO for state of external inputs IN 1..4 disabled 1 = FIFO for state of external inputs IN 1..4 enabled
9	0 = FIFO for state of RxD inputs (sensor 1..6) disabled 1 = FIFO for state of RxD inputs (sensor 1..6) enabled
10	0 = FIFO for ADC 1 disabled 1 = FIFO for ADC 1 enabled
11	0 = FIFO for ADC 2 disabled 1 = FIFO for ADC 2 enabled
12	0 = FIFO is disabled for sensor 1 and 2 if ext. input IN 1 is active 1 = IN 1 does not affect FIFO
13	0 = FIFO is disabled for sensor 3 and 6 if ext. input IN 2 is active 1 = IN 2 does not affect FIFO
14	0 = FIFO is disabled for encoder 1 and 2 if ext. input IN 3 is active 1 = IN 3 does not affect FIFO
15	0 = FIFO is disabled for ADC 1/2; IN 1..4; RxD 1..6 if ext. input IN 4 is active 1 = IN 4 does not affect FIFO

Table 15: FIFO enable register

5.6 Interrupt Enable Register

Base addr. + 06h (write access)

Bit	Function
0	1 = Enable interrupt requirements if FIFO is filled with more than 50 %
1	1 = Enable interrupt requirements if FIFO is filled with more than 75 %
2	1 = Enable interrupt requirements on overflow Timer 1
3	1 = Enable interrupt requirements on overflow Timer 2
4	1 = Enable interrupt requirements on overflow Timer 3
5	1 = Enable interrupt requirements if external input IN 1 is activated
6	1 = Enable interrupt requirements if external input IN 2 is activated
7	1 = Enable interrupt requirements if external input IN 3 is activated
8	1 = Enable interrupt requirements if external input IN 4 is activated
9 - 15	Reserved

Table 16: Interrupt enable register

Please note:

The interrupt generation is controlled by a trigger flange, i.e., an interrupt requirement is only effected if the corresponding bit is set in the interrupt enable register. Furthermore, the appropriate source has to change from the inactive into the active state. Several bits can be set at the same time.

5.7 Interrupt Status Register

Base addr. + 06h (read access)

Bit	Function
0	1 = Interrupt requirement if FIFO level exceeds 50%
1	1 = Interrupt requirement if FIFO level exceeds 75%
2	1 = Interrupt requirement on overflow Timer 1
3	1 = Interrupt requirement on overflow Timer 2
4	1 = Interrupt requirement on overflow Timer 3
5	1 = Interrupt requirement if external input IN 1 is activated
6	1 = Interrupt requirement if external input IN 2 is activated
7	1 = Interrupt requirement if external input IN 3 is activated
8	1 = Interrupt requirement if external input IN 4 is activated
9 - 15	Reserved

Table 17: Interrupt status register

Please note:

The interrupt state register informs by which source(s) the interrupt requirements have been generated. One interrupt requirement can be effected by using more than one source at the same time. In case that no state bit is set, the interrupt requirement was not generated by the IF2008A but by another hardware.

5.8 Sensor Baud Rate

Base addr.	Sensor channel	Value	Access
+ 08h	1	1 to 65,535	only write access
+ 0Ah	2	1 to 65,535	only write access
+ 0Ch	3	1 to 65,535	only write access
+ 0Eh	4	1 to 65,535	only write access
+ 10h	5	1 to 65,535	only write access
+ 12h	6	1 to 65,535	only write access

Table 18: Base addresses for sensor baud rates

Value = (48 MHz / baud rate) – 1

Example:

Desired baud rate = 691.2 kBaud

Value = (48 MHZ / 691,200) - 1 = 68.44

The input value must be a whole number, i.e., the result must still be rounded:

➔ **Value = 68**

5.9 Counter Control Register

Base addr.	Counter channel	Bit	Access
+ 14h	1	0 to 15	Read and write access
+ 16h	2	0 to 15	Read and write access

Table 19: Base addresses for counter control register

The tables below are the same for both counter channels!

Overview of Functions

Bit	Function
0 to 3	Interpolation (see Table 21: Encoder interpolation)
4	Counting direction (see Table 22: Encoder counter direction)
5 to 7	Counter mode (see Table 23: Counter mode)
8 to 11	Latch source (see Table 24: Counter latch source)
12 to 15	Reserved

Table 20: Functional overview for counter control register

Interpolation

Bit 3	Bit 2	Bit 1	Bit 0	Interpolation
0	0	0	0	1
0	0	0	1	2
0	0	1	0	3
0	0	1	1	4
0	1	0	0	5
0	1	0	1	6
0	1	1	0	8
0	1	1	1	10
1	0	0	0	12
1	0	0	1	16
1	0	1	0	20
1	0	1	1	24
1	1	0	0	32
1	1	0	1	40
1	1	1	0	48
1	1	1	1	64

Table 21: Encoder interpolation

Please note:

- For encoders with 1-Vss signals all interpolations are suitable
- For encoders with TTL-signals the following interpolations are suitable: 1, 2 or 4 times

Counting direction

Bit 4	Counting direction
0	normal
1	inversed

Table 22: Encoder counter direction

Counter mode:

Bit 7	Bit 6	Bit 5	Counter mode
0	0	0	No counter load / delete function by encoder reference marker
0	0	1	Counter is loaded with the next encoder reference marker provided that the state bit 0 or state bit 2 “0” is settled.
0	1	0	Counter is loaded including all encoder reference markers and load register content. State bit 0 to 3 have no effect.
0	1	1	Counter is deleted including all encoder reference markers and additionally loaded with the content of the load register if the counter has reached -1. This function offers the possibility to limit the counter. During this process the counter load register has to be preallocated with the number of increments limited -1.
1	0	0	Counter without phase discriminator (event counter) Bit 4 / Function: 0: Track A = counter direction signal 0: Track B = counter clock signal 1: Track A = counter clock signal 1: Track B = counter direction signal
1	0	1	Reserved
1	1	0	Reserved
1	1	1	Reserved

Table 23: Counter mode

Latch source:

Bit 11	Bit 10	Bit 9	Bit 8	Latch source
0	0	0	0	Hardware latch disabled
0	0	0	1	Timer 1
0	0	1	0	Timer 2
0	0	1	1	Timer 3
0	1	0	0	Sensor channel 1
0	1	0	1	Sensor channel 2
0	1	1	0	Sensor channel 3
0	1	1	1	Sensor channel 4
1	0	0	0	Sensor channel 5
1	0	0	1	Sensor channel 6
1	0	1	0	IN 1 (only with IF2008E expansion board)
1	0	1	1	IN 2 (only with IF2008E expansion board)
1	1	0	0	IN 3 (only with IF2008E expansion board)
1	1	0	1	IN 4 (only with IF2008E expansion board)
1	1	1	0	2nd reference mark
1	1	1	1	all reference marks

Table 24: Counter latch source

5.10 Counter Preload

Base addr.	Counter channel	Value	Access
+ 18h	1 LSW	0 to 65,535	only write access
+ 1Ah	1 MSW	0 to 65,535	only write access
+ 1Ch	2 LSW	0 to 65,535	only write access
+ 1Eh	2 MSW	0 to 65,535	only write access

Table 25: Base addresses for counter preload

5.11 Counter Value

Base addr.	Counter channel	Value	Access
+ 18h	1 LSW	0 to 65,535	only read access
+ 1Ah	1 MSW	0 to 65,535	only read access
+ 1Ch	2 LSW	0 to 65,535	only read access
+ 1Eh	2 MSW	0 to 65,535	only read access

Table 26: Base addresses for counter value

5.12 Timer

Base addr.	Timer	Value	Access
+ 20h	1 frequency	0 to 65,535	only write access
+ 22h	1 pulse width	0 to 65,535	only write access
+ 24h	2 frequency	0 to 65,535	only write access
+ 26h	2 pulse width	0 to 65,535	only write access
+ 28h	3 frequency	0 to 65,535	only write access
+ 2Ah	3 pulse width	0 to 65,535	only write access
+ 2Ch	Clock splitter		Read and write access

Table 27: Base addresses for timer

$$\mathbf{Value(F) = (F_{Clock} / F_{OUT}) - 1}$$

$$\mathbf{Value(PW) = (PW_{OUT} / T_{Clock})}$$

Example:

Desired frequency F_{OUT} = 10 kHz

Desired pulse width PW_{OUT} = 25 µs

Clock splitter = 0 → F_{Clock} = 24 MHZ, T_{Clock} = 41.667 ns (see the following table for clock splitter)

Value(F) = (24 MHZ / 10 kHz) - 1 = 2399

Value(PW) = (25 µs / 41.667 ns) = 600

The input values must be whole numbers!

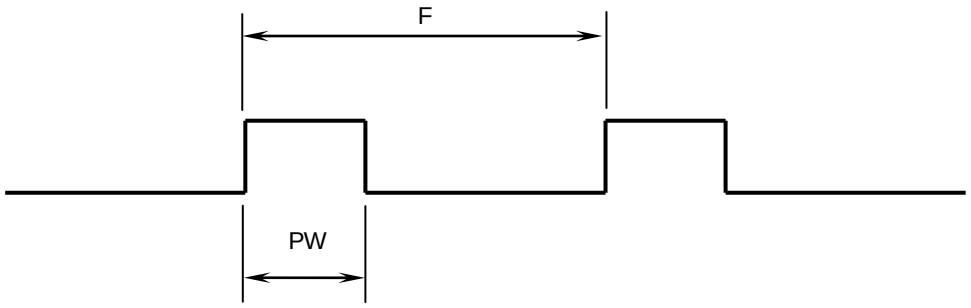


Figure 5: Timer frequency and pulse width

Please note:

The pulse width only affects the “sensor trigger” and “optocoupler” outputs and not the internal synchronization signals. For this, the zero crossing timer is used.

To turn off the timer, the frequency must be programmed to be "0". If pulse width > 0 is programmed when the timer is turned off, output is permanently set to High. However, if the pulse width is also programmed to be "0", output is permanently set to Low.

Clock Splitter:

Bit 3	Bit 2	Bit 1	Bit 0	Clock frequency timer 1
Bit 7	**Bit 6**	**Bit 5**	**Bit 4**	**Clock frequency timer 2**
Bit 11	**Bit 10**	**Bit 9**	**Bit 8**	**Clock frequency timer 3**
0	0	0	0	24 MHz
0	0	0	1	24 MHz / 2
0	0	1	0	24 MHz / 4
0	0	1	1	24 MHz / 8
0	1	0	0	24 MHz / 16
0	1	0	1	24 MHz / 32
0	1	1	0	24 MHz / 64
0	1	1	1	24 MHz / 128
1	0	0	0	24 MHz / 256
1	0	0	1	24 MHz / 512
1	0	1	0	24 MHz / 1024
1	0	1	1	24 MHz / 2048
1	1	0	0	24 MHz / 4096
1	1	0	1	24 MHz / 8192
1	1	1	0	24 MHz / 16384
1	1	1	1	24 MHz / 32768

Table 28: Timer clock splitter

Please note:
Bit 12 to Bit 15 are reserved.

5.13 ADC

Base addr.	ADC channel	Value	Access
+ 20h	1	0 to 65535	only read access
+ 22h	2	0 to 65535	only read access

Table 29: Base addresses for ADC

5.14 State

Base addr. + 24h (only read access)

Bit	Function
0	1 = Encoder 1: 1st reference mark crossed
1	1 = Encoder 1: 2nd reference mark crossed
2	1 = Encoder 2: 1st reference mark crossed
3	1 = Encoder 2: 2nd reference mark crossed
4	0 = Transmitter ready for new data transfer 1 = Transmitter is occupied
5	0 = No extension module with sensor 5 / 6 available 1 = Extension module with sensor 5 / 6 available
6	0 = No extension module for external I/O available 1 = Extension module for external I/O available
7	0 = No extension module with ADC available 1 = Extension module with ADC available
8 – 13	FPGA version
14 – 15	Hardware version

Table 30: Status

5.15 Input and Sensor Power Switch Status

Base addr. + 26h (only read access)

Bit	Function
0	1 = Ext. input IN 1 active
1	1 = Ext. input IN 2 active
2	1 = Ext. input IN 3 active
3	1 = Ext. input IN 4 active
4	1 = RxD input on the sensor input 1 active
5	1 = RxD input on the sensor input 2 active
6	1 = RxD input on the sensor input 3 active
7	1 = RxD input on the sensor input 4 active
8	1 = RxD input on the sensor input 5 active
9	1 = RxD input on the sensor input 6 active
10	1 = Error sensor power switch
11 – 15	Reserved

Table 31: Input und sensor power switch

5.16 Output Register

Base addr. + 2Eh (read and write access)

Bit	Function			Output signal	
0	0 = OUT 1 OFF 1 = OUT 1 ON	Optocoupler disabled Optocoupler conductive	[1]	Output 1 = High Output 1 = Low	
1	0 = OUT 2 OFF 1 = OUT 2 ON	Optocoupler disabled Optocoupler conductive	[1]	Output 2 = High Output 2 = Low	
2	0 = OUT 3 OFF 1 = OUT 3 ON	Optocoupler disabled Optocoupler conductive	[1]	Output 3 = High Output 3 = Low	
3	0 = OUT 4 OFF 1 = OUT 4 ON	Optocoupler disabled Optocoupler conductive	[1]	Output 4 = High Output 4 = Low	
4	0 = TxD 1 1 = TxD 1	inactive active		TxD 1+ = High TxD 1+ = Low	TxD 1- = Low TxD 1- = High
5	0 = TxD 2 1 = TxD 2	inactive active		TxD 2+ = High TxD 2+ = Low	TxD 2- = Low TxD 2- = High
6	0 = TxD 3 1 = TxD 3	inactive active		TxD 3+ = High TxD 3+ = Low	TxD 3- = Low TxD 3- = High
7	0 = TxD 4 1 = TxD 4	inactive active		TxD 4+ = High TxD 4+ = Low	TxD 4- = Low TxD 4- = High
8	0 = TxD 5 1 = TxD 5	inactive active	[1]	TxD 5+ = High TxD 5+ = Low	TxD 5- = Low TxD 5- = High
9	0 = TxD 6 1 = TxD 6	inactive active	[1]	TxD 6+ = High TxD 6+ = Low	TxD 6- = Low TxD 6- = High
10	0 = TRG 1 1 = TRG 1	inactive active		TRG 1+ = Low TRG 1+ = High	TRG 1- = High TRG 1- = Low
11	0 = TRG 2 1 = TRG 2	inactive active		TRG 2+ = Low TRG 2+ = High	TRG 2- = High TRG 2- = Low
12	0 = TRG 3 1 = TRG 3	inactive active		TRG 3+ = Low TRG 3+ = High	TRG 3- = High TRG 3- = Low
13	0 = TRG 4 1 = TRG 4	inactive active		TRG 4+ = Low TRG 4+ = High	TRG 4- = High TRG 4- = Low
14	0 = TRG 5 1 = TRG 5	inactive active	[1]	TRG 5+ = Low TRG 5+ = High	TRG 5- = High TRG 5- = Low
15	0 = TRG 6 1 = TRG 6	inactive active	[1]	TRG 6+ = Low TRG 6+ = High	TRG 6- = High TRG 6- = Low

Table 32: Output register

Please note:

For all outputs, several signal sources are available. Bits listed above are only connected through in case that the appropriate mode is set (see Table 33: Mode Opto- and TxD Outputs on page 22).

[1] Possible only with expansion board

5.17 Mode Opto- and TxD Outputs

Base addr. + 30h (read and write access)

<table>
<tr><th>Bit</th><th>Function</th></tr>
<tr><td>0 and 1</td><td>
<table>
<tr><th>Bit 1</th><th>Bit 0</th><th>Function</th></tr>
<tr><td>0</td><td>0</td><td>Output 1 switches Bit 0 with addr. 2Eh</td></tr>
<tr><td>0</td><td>1</td><td>Output 1 switches pulse width with Timer 1</td></tr>
<tr><td>1</td><td>0</td><td>Output 1 switches pulse width with Timer 2</td></tr>
<tr><td>1</td><td>1</td><td>Output 1 switches pulse width with Timer 3</td></tr>
</table>
</td></tr>
<tr><td>2 and 3</td><td>
<table>
<tr><th>Bit 3</th><th>Bit 2</th><th>Function</th></tr>
<tr><td>0</td><td>0</td><td>Output 2 switches Bit 1 with addr. 2Eh</td></tr>
<tr><td>0</td><td>1</td><td>Output 2 switches pulse width with Timer 1</td></tr>
<tr><td>1</td><td>0</td><td>Output 2 switches pulse width with Timer 2</td></tr>
<tr><td>1</td><td>1</td><td>Output 2 switches pulse width with Timer 3</td></tr>
</table>
</td></tr>
<tr><td>4 and 5</td><td>
<table>
<tr><th>Bit 5</th><th>Bit 4</th><th>Function</th></tr>
<tr><td>0</td><td>0</td><td>Output 3 switches Bit 2 with addr. 2Eh</td></tr>
<tr><td>0</td><td>1</td><td>Output 3 switches pulse width with Timer 1</td></tr>
<tr><td>1</td><td>0</td><td>Output 3 switches pulse width with Timer 2</td></tr>
<tr><td>1</td><td>1</td><td>Output 3 switches pulse width with Timer 3</td></tr>
</table>
</td></tr>
<tr><td>6 and 7</td><td>
<table>
<tr><th>Bit 7</th><th>Bit 6</th><th>Function</th></tr>
<tr><td>0</td><td>0</td><td>Output 4 switches Bit 3 with addr. 2Eh</td></tr>
<tr><td>0</td><td>1</td><td>Output 4 switches pulse width with Timer 1</td></tr>
<tr><td>1</td><td>0</td><td>Output 4 switches pulse width with Timer 2</td></tr>
<tr><td>1</td><td>1</td><td>Output 4 switches pulse width with Timer 3</td></tr>
</table>
</td></tr>
<tr><td>8</td><td>0 = TxD 1 switches with transmitter
1 = TxD 1 switches bit 4 with addr. 2Eh</td></tr>
<tr><td>9</td><td>0 = TxD 2 switches with transmitter
1 = TxD 2 switches bit 5 with addr. 2Eh</td></tr>
<tr><td>10</td><td>0 = TxD 3 switches with transmitter
1 = TxD 3 switches bit 6 with addr. 2Eh</td></tr>
<tr><td>11</td><td>0 = TxD 4 switches with transmitter
1 = TxD 4 switches bit 7 with addr. 2Eh</td></tr>
<tr><td>12</td><td>0 = TxD 5 switches with transmitter
1 = TxD 5 switches bit 8 with addr. 2Eh</td></tr>
<tr><td>13</td><td>0 = TxD 6 switches with transmitter
1 = TxD 6 switches bit 9 with addr. 2Eh</td></tr>
<tr><td>14 - 15</td><td>Reserved</td></tr>
</table>

Table 33: Mode Opto- and TxD Outputs

Please note:

The outputs 1 to 4 are only available for the IF2008E expansion board.

5.18 Mode Trigger Outputs, Latch Source and Sensor Power Switch

Base addr. + 32h (read and write access)

Bit	Function
0 and 1	

Bit 1	Bit 0	Function
0	0	Trigger 1 switches Bit 10 with addr. 2Eh
0	1	Trigger 1 switches pulse width with Timer 1
1	0	Trigger 1 switches pulse width with Timer 2
1	1	Trigger 1 switches pulse width with Timer 3

2 and 3

Bit 3	Bit 2	Function
0	0	Trigger 2 switches Bit 11 with addr. 2Eh
0	1	Trigger 2 switches pulse width with Timer 1
1	0	Trigger 2 switches pulse width with Timer 2
1	1	Trigger 2 switches pulse width with Timer 3

4 and 5

Bit 5	Bit 4	Function
0	0	Trigger 3 switches Bit 12 with addr. 2Eh
0	1	Trigger 3 switches pulse width with Timer 1
1	0	Trigger 3 switches pulse width with Timer 2
1	1	Trigger 3 switches pulse width with Timer 3

6 and 7

Bit 7	Bit 6	Function
0	0	Trigger 4 switches Bit 13 with addr. 2Eh
0	1	Trigger 4 switches pulse width with Timer 1
1	0	Trigger 4 switches pulse width with Timer 2
1	1	Trigger 4 switches pulse width with Timer 3

8 and 9

Bit 9	Bit 8	Function
0	0	Trigger 5 switches Bit 14 with addr. 2Eh
0	1	Trigger 5 switches pulse width with Timer 1
1	0	Trigger 5 switches pulse width with Timer 2
1	1	Trigger 5 switches pulse width with Timer 3

10 and 11

Bit 11	Bit 10	Function
0	0	Trigger 6 switches Bit 15 with addr. 2Eh
0	1	Trigger 6 switches pulse width with Timer 1
1	0	Trigger 6 switches pulse width with Timer 2
1	1	Trigger 6 switches pulse width with Timer 3

<table>
<tr><th>Bit</th><th>Function</th></tr>
<tr><td>12 – 14</td><td>
<table>
<tr><th>Bit 14</th><th>Bit 13</th><th>Bit 12</th><th>Latch source</th></tr>
<tr><td>0</td><td>0</td><td>0</td><td>Hardware latch disabled</td></tr>
<tr><td>0</td><td>0</td><td>1</td><td>Timer 1</td></tr>
<tr><td>0</td><td>1</td><td>0</td><td>Timer 2</td></tr>
<tr><td>0</td><td>1</td><td>1</td><td>Timer 3</td></tr>
<tr><td>1</td><td>0</td><td>0</td><td>Sensor channel 1</td></tr>
<tr><td>1</td><td>0</td><td>1</td><td>Sensor channel 2</td></tr>
<tr><td>1</td><td>1</td><td>0</td><td>Sensor channel 3</td></tr>
<tr><td>1</td><td>1</td><td>1</td><td>Sensor channel 4</td></tr>
</table>
</td></tr>
<tr><td>15</td><td>Bit 15 = 0 Sensor power ON (default value after Reset)
Bit 15 = 1 Sensor power OFF</td></tr>
</table>

Table 34: Mode trigger outputs, latch source and sensor power switch

Please note:

Bits 12 to 14 can be used to select a latch source whose trigger event writes the external trigger inputs (IN 1 to 4) and the RxD inputs (sensor 1 to 6) to FIFO.

5.19 ADC Control Register

Base addr. + 34h (read and write access)

Bit 3	Bit 2	Bit 1	Bit 0	Conversion source ADC1
Bit 7	**Bit 6**	**Bit 5**	**Bit 4**	**Conversion source ADC2**
0	0	0	0	Hardware conversion disabled
0	0	0	1	Timer 1
0	0	1	0	Timer 2
0	0	1	1	Timer 3
0	1	0	0	Sensor channel 1
0	1	0	1	Sensor channel 2
0	1	1	0	Sensor channel 3
0	1	1	1	Sensor channel 4
1	0	0	0	Sensor channel 5
1	0	0	1	Sensor channel 6
1	0	1	0	IN 1 (only with IF2008E expansion board)
1	0	1	1	IN 2 (only with IF2008E expansion board)
1	1	0	0	IN 3 (only with IF2008E expansion board)
1	1	0	1	IN 4 (only with IF2008E expansion board)
1	1	1	0	Reserved
1	1	1	1	Reserved

Table 35: ADC control register bits 0-7

Bit	Function
8	0 = ADC1 data output binary 2-complement 1 = ADC1 data output binary unconverted
9	0 = ADC2 data output binary 2-complement 1 = ADC2 data output binary unconverted
10 – 15	Reserved

Table 36: ADC control register bits 8-15

Analog input				Digital output	
0 – 5 V	0 – 10 V	+/-5 V	+/-10 V	Binary 2-complement	Binary unconverted
+4.99V	+9.99V	+4.99V	+9.99V	7FFF	FFFF
2.5V	5V	0V	0V	0000	8000
+2.499V	+4.999V	-153 µV	-305 µV	FFFF	7FFF
0V	0V	-5V	-10V	8000	0000

Table 37: ADC converting result

5.20 Parity Enable Register

Base addr. + 36h (write access)

Bit	Function
0	0 = Parity bit for sensor channel 1 disabled 1 = Parity bit for sensor channel 1 enabled (only even parity)
1	0 = Parity bit for sensor channel 2 disabled 1 = Parity bit for sensor channel 2 enabled (only even parity)
2	0 = Parity bit for sensor channel 3 disabled 1 = Parity bit for sensor channel 3 enabled (only even parity)
3	0 = Parity bit for sensor channel 4 disabled 1 = Parity bit for sensor channel 4 enabled (only even parity)
4	0 = Parity bit for sensor channel 5 disabled 1 = Parity bit for sensor channel 5 enabled (only even parity)
5	0 = Parity bit for sensor channel 6 disabled 1 = Parity bit for sensor channel 6 enabled (only even parity)
6-15	Reserved

Table 38: Parity enable register

5.21 Parity Error Register

Base addr. + 36h (read access)

Bit	Function
0	1 = Parity-Error sensor channel 1
1	1 = Parity-Error sensor channel 2
2	1 = Parity-Error sensor channel 3
3	1 = Parity-Error sensor channel 4
4	1 = Parity-Error sensor channel 5
5	1 = Parity-Error sensor channel 6
6 – 15	Reserved

Table 39: Parity error register

6 Wiring Recommendations

6.1 Sensor ILD1420

Pin IF2008/PCIe	Signal IF2008/PCIe	ILD1420		Signal ILD1420
		Pin Sensor 1	Pin Sensor 2	
1	Sensor 1 TxD-	4		RxD-
2	Sensor 1 TxD+	3		RxD+
3	Sensor 1 RxD-	6		TxD-
4	Sensor 1 RxD+	5		TxD+
5	Power supply 0V	12	12	GND
6	Sensor 1 TRG+	9		TeachIn
7	Sensor 1 TRG-	n.c.	n.c.	
8	Sensor 2 TRG+		9	TeachIn
9	Sensor 2 TRG-	n.c.	n.c.	
10	Power supply +24V	7	7	+UB
11	Sensor 2 TxD-		4	RxD-
12	Sensor 2 TxD+		3	RxD+
13	Sensor 2 RxD-		6	TxD-
14	Sensor 2 RxD+		5	TxD+
15	GND (galvanically separated to GND PC)	12	12	GND

Table 40: Sensor wiring ILD1420

6.2 Sensor ILD1750

Pin IF2008/PCIe	Signal IF2008/PCIe	ILD1750		Signal ILD1750
		Pin Sensor 1	Pin Sensor 2	
1	Sensor 1 TxD-	11		RxD-
2	Sensor 1 TxD+	12		RxD+
3	Sensor 1 RxD-	2		TxD-
4	Sensor 1 RxD+	1		TxD+
5	Power supply 0V	6	6	GND
6	Sensor 1 TRG+	3		TRG+
7	Sensor 1 TRG-	4		TRG-
8	Sensor 2 TRG+		3	TRG+
9	Sensor 2 TRG-		4	TRG-
10	Power supply +24V	5	5	+UB
11	Sensor 2 TxD-		11	RxD-
12	Sensor 2 TxD+		12	RxD+
13	Sensor 2 RxD-		2	TxD-
14	Sensor 2 RxD+		1	TxD+
15	GND (galvanically separated to GND PC)	6	6	GND

Table 41: Sensor wiring ILD1750

6.3 Sensor ILD2300

Pin IF2008/PCIe	Signal IF2008/PCIe	ILD2300		Signal ILD2300
		Pin Sensor 1	Pin Sensor 2	
1	Sensor 1 TxD-	8		RxD-
2	Sensor 1 TxD+	7		RxD+
3	Sensor 1 RxD-	10		TxD-
4	Sensor 1 RxD+	9		TxD+
5	Power supply 0V	2	2	Supply ground
6	Sensor 1 TRG+	5		SyncIn+
7	Sensor 1 TRG-	6		
8	Sensor 2 TRG+		5	SyncIn+
9	Sensor 2 TRG-		6	
10	Power supply +24V	1	1	+UB
11	Sensor 2 TxD-		8	RxD-
12	Sensor 2 TxD+		7	RxD+
13	Sensor 2 RxD-		10	TxD-
14	Sensor 2 RxD+		9	TxD+
15	GND (galvanically separated to GND PC)	2	2	SyncIn-

Table 42: Sensor wiring ILD2300

6.4 Encoder Interface

Pin IF2008/PCIe	Signal IF2008/PCIe	1Vss or RS422		TTL (single-ended)	
		Signal Encoder 1	Signal Encoder 2	Signal Encoder 1	Signal Encoder 2
1	Encoder 1 Track A+	A+		A	
2	Encoder 1 Track A-	A-		open	
3	Encoder 2 Track A+		A+		A
4	Encoder 2 Track A-		A-		open
5	VCC (+5 V)	+UB	+UB	+UB	+UB
6	Encoder 1 Track B+	B+		B	
7	Encoder 1 Track B-	B-		open	
8	Encoder 2 Track B+		B+		B
9	Encoder 2 Track B-		B-		open
10	GND	GND	GND	GND	GND
11	Encoder 1 Track R+	R+		R	
12	Encoder 1 Track R-	R-		open	
13	Encoder 2 Track R+		R+		R
14	Encoder 2 Track R-		R-		open
15	GND	GND	GND	GND	GND

Table 43: Encoder interface

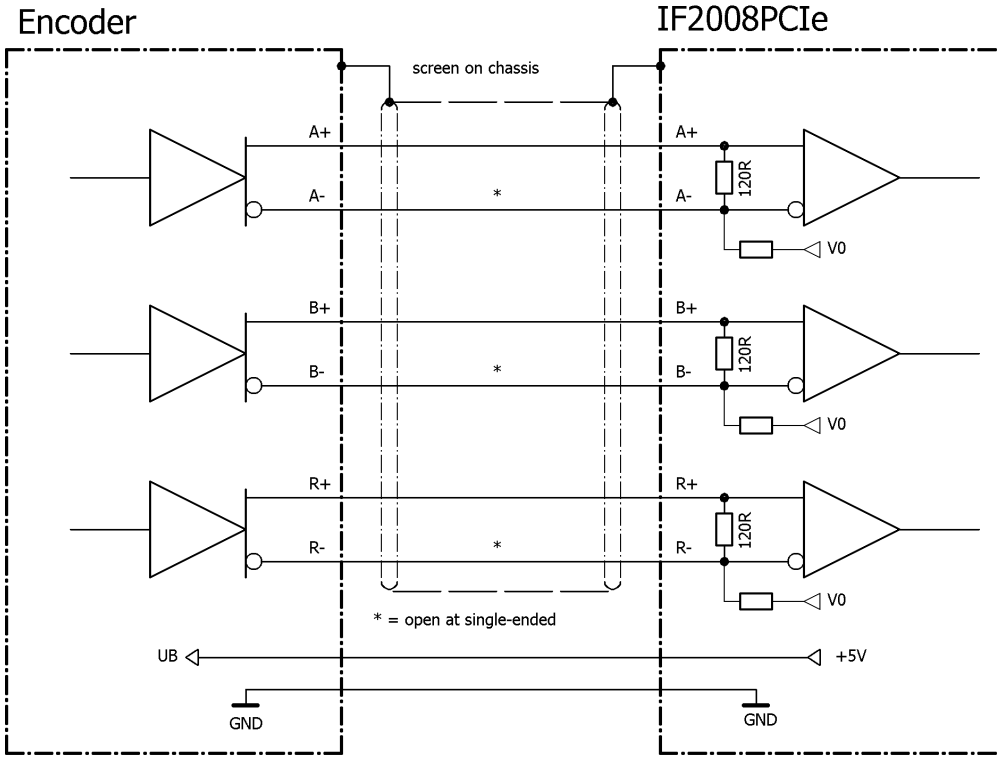


Figure 6: Block diagram encoder interface

Please note:
Plus inputs (A+, B+, R+) may not remain open. For example, if only the clock signal is used, the plus inputs have to be set on GND or VCC.

6.5 Optocoupler I/O

Pin IF2008/PCIe	Signal IF2008/PCIe
1	OUT1
2	OUT2
3	OUT3
4	OUT4
5	GND
6	IN1
7	IN2
8	IN3
9	IN4

Table 44: Optocoupler I/O

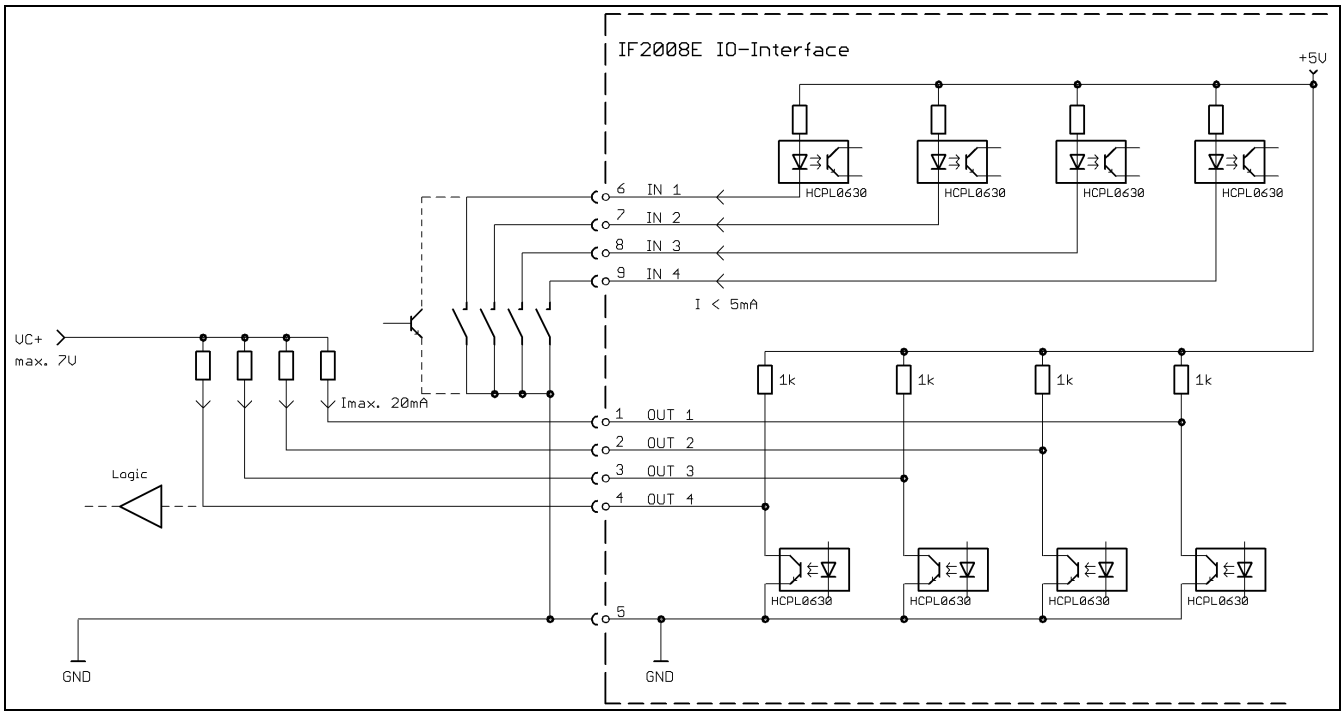


Figure 7: Block diagram optocoupler I/O

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MICRO-EPSILON

Manual

IF2008A PCI Basis Board
IF2008E Expansion Board

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1 Technical Data

1.1 IF2008A Basic Printed Circuit Board

Mechanics and Environment

- Dimensions (circuit board) approx. 140 x 102 mm, 1 slot wide
- Ambient temperature +50°C maximum
- 2x D-SUB female connectors HD 15-pin for sensor connections
- 1x D-SUB male connector HD 15-pin for encoder signals
- Tyco/AMP Commercial MATE-N-LOK connector (IDE hard drive connector) for supply DC-/DC converter
- 3x female connectorss Tyco/AMP MicroMatch for connection to IF2008E

PCI-Bus

- PCI connector 3.3 or 5 Volt 32 bit 2x60 pin
- Target interface (slave) according to specifications Rev. 2.1 and 2.2
- Bus clock frequency 40 MHz maximum
- Current consumption +5 Volt approx. 0.5 A, sensors and encoder excluded

Sensor Interface (X1 / X2)

- 2 RS422 driver and two RS422 receiver including galvanic isolation per connector (in- / output frequency 5 MHz maximum)
- 2 LVDS or 3.3 Volt CMOS outputs including galvanic isolation per connector (output frequency 5 MHz maximum)
- Power supply of the sensors 24 V

Encoder Interface (X3)

- Interface for two encoders with 1 V_{ss}-, RS422- (differential-) or TTL- (single-ended) signals
- Power supply of the encoders with +5 V, PCI supply without galvanic isolation (current consumption depends on encoders connected)
- Interpolation programmable from 1- to 64 times in case of encoders with 1 V_{ss} signals (input frequency maximum = [3.2 MHz / interpolation] ≤ 800 kHz)
- Evaluation programmable from 1- to 4-times in case of encoders with:
  RS422- / differential signal (input frequency max. = 800 kHz)
  TTL- / single-ended signals (input frequency max. = 400 kHz)

DC-/DC-Converter

- Input voltage range 12 V ±1.0 V
- Output voltage 24 V ±0.5 V
- Output current 1.25 A max. for all sensors
- Efficiency typical 90 %

The supply of the DC-DC converter with power supply within the computer. The connection between the PC power supply and the IF2008A has to be done during the installation of the card.

1.2 IF2008E Expansion Board

Mechanics and Environment

- Dimensions (conductor board) approx. 71 x 102 mm, 1 slot wide
- Ambient temperature +50 °C maximum
- 1x D-SUB female connector HD 15-pin for sensor connections
- 1x D-SUB female connector 9-pin for I/O-Interface
- 1x D-SUB male connector 9-pin for analog inputs
- 3x female connectors MicroMatch for connection to IF2008A

Sensor Interface (X1)

- Similar to IF2008A (X1)

I/O Interface (X2)

- 4 optocoupler inputs, current input 5 mA maximum, input frequency 1 MHz maximum
- 4 optocoupler outputs, current output 20 mA maximum, output frequency 1 MHz maximum

Analog Interface (X3)

- 2x ADC channels
- Input voltage range 0-5 V, 0-10 V, ±5 V, ±10 V adjustable separately for each channel by means of DIP switch
- Resolution 16 bit
- Offset error ±3 mV maximum
- Gain error ±5 mV maximum
- Conversion rate 150 kHz mximum per channel

2 Hardware

2.1 View IF2008A

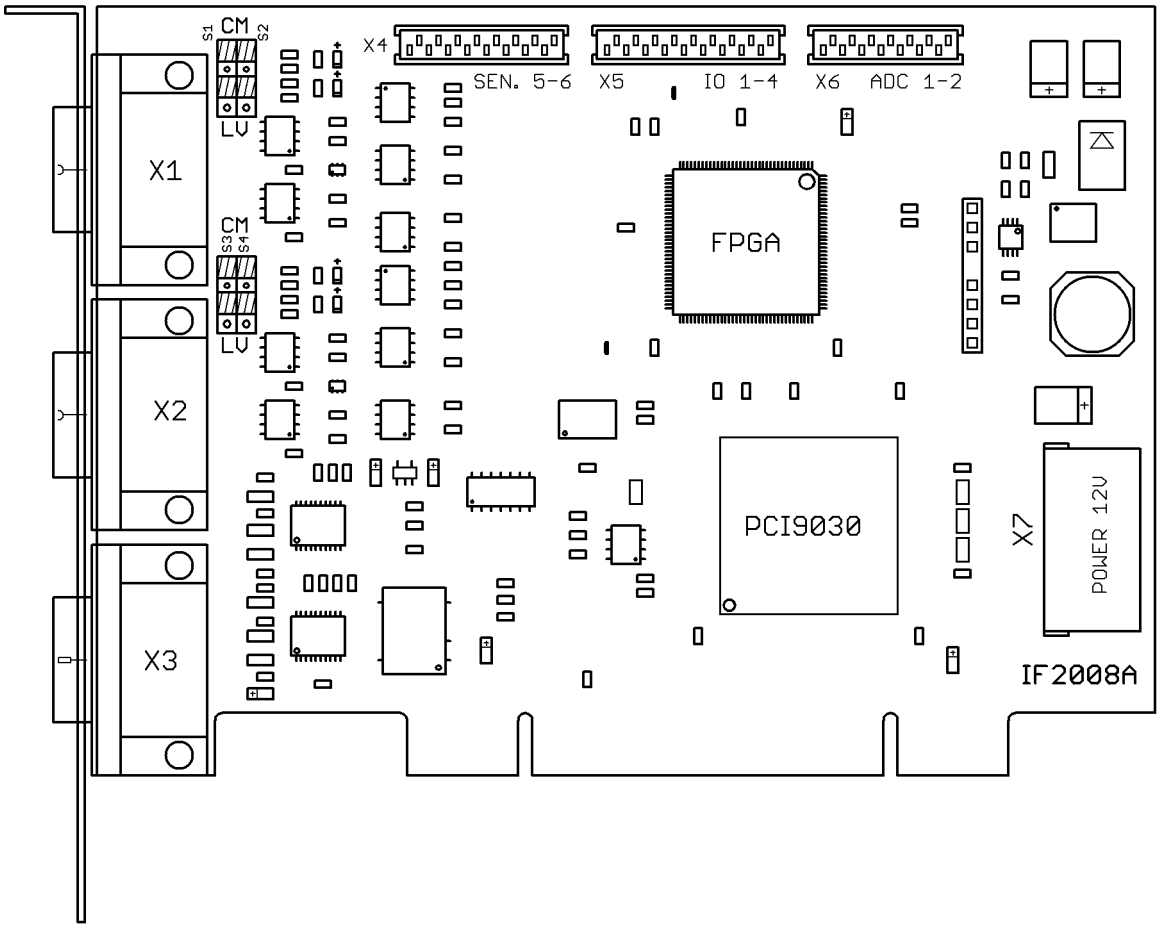


Image 1: View of board IF2008A

- X1 = Sensor connection 1 and 2
- X2 = Sensor connection 3 and 4
- X3 = Encoder connection 1 and 2
- X4 ... X6 = Connection to IF2008E
- X7 = Connection 12 V power, connection to the power supply required
- S1 .. S4 = Switch for positive trigger level

2.2 View IF2008E

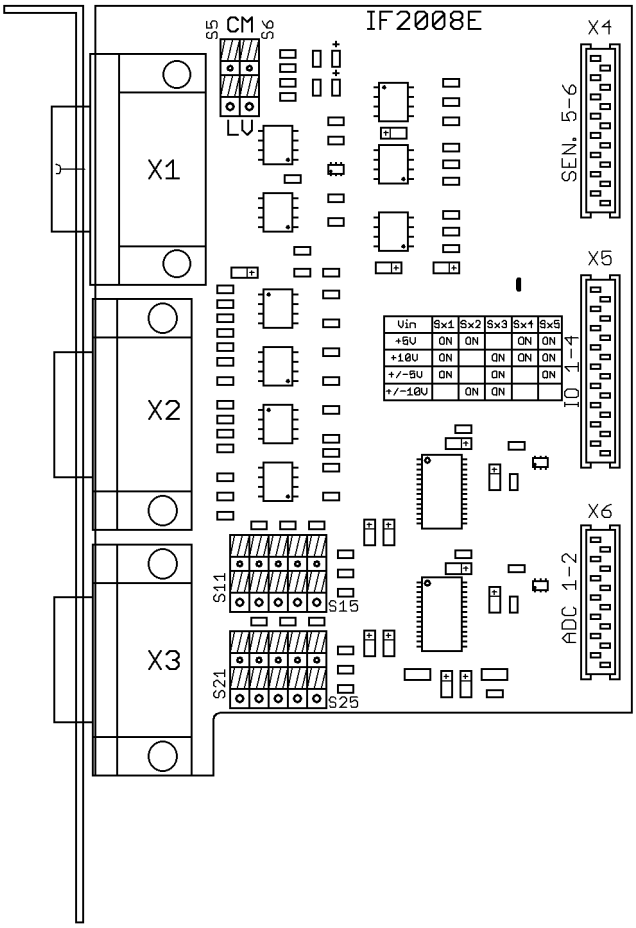


Image 2: View of board IF2008A

- X1 = Sensor connection 5 and 6
- X2 = Connection for I/O signals
- X3 = Connection to analog digital converter
- X4 ... X6 = Connection to IF2008A
- S5 u. S6 = Switch for positive trigger level
- S11 ... S15 = Switch for ADC level 1
- S21 ... S25 = Switch for ADC level 2

3 Pin Assignments and Jumper Setting

3.1 Sensor Interface (IF2008A X1 and X2, IF2008E X1)

Pin	Signal
1	Sensor 1 TxD-
2	Sensor 1 TxD+
3	Sensor 1 RxD-
4	Sensor 1 RxD+
5	Power supply 0V
6	Sensor 1 TRG+
7	Sensor 1 TRG-
8	Sensor 2 TRG+
9	Sensor 2 TRG-
10	Power supply +24V
11	Sensor 2 TxD-
12	Sensor 2 TxD+
13	Sensor 2 RxD-
14	Sensor 2 RxD+
15	GND (galvanic isolation to PC-GND)

Table 1: Pin assignment sensor interface

3.2 Encoder Interface (IF2008A X3)

Pin	Function
1	Encoder 1 track A+
2	Encoder 1 track A-
3	Encoder 2 track A+
4	Encoder 2 track A-
5	VCC (+5V)
6	Encoder 1 track B+
7	Encoder 1 track B-
8	Encoder 2 track B+
9	Encoder 2 track B-
10	GND
11	Encoder 1 track R+
12	Encoder 1 track R-
13	Encoder 2 track R+
14	Encoder 2 track R-
15	GND

Table 2: Pin assignment encoder interface

Attention: The pin assignment is not compatible with IF2004B!

3.3 Sensor Power (IF2008A X7)

Pin	Function
1	+12 V
2	GND
3	GND
4	NC

Table 3: Pin assignment sensor power

3.4 I/O Interface (IF2008E X2)

Pin	Function
1	OUT 1
2	OUT 2
3	OUT 3
4	OUT 4
5	GND (galvanic isolation to PC-GND)
6	IN 1
7	IN 2
8	IN 3
9	IN 4

Table 4: Pin assignment I/O interface

3.5 Analog Interface (IF2008E X3)

Pin	Function
1	Input signal 1
2	Analog GND
3	Input signal 2
4	Analog GND
5	NC
6	NC
7	NC
8	NC
9	NC

Table 5: Pin assignment analog interface

3.6 Jumper-/Switch Setting for Trigger Level

By means of the switches S1 to S4 (IF2008A) and the switches S5 and S6 (IF2008E) the positive trigger level for the sensor channels 1 to 4 (IF2008A) or 5 and 6 (IF2008E) can be selected. The negative output always has LVDS level.

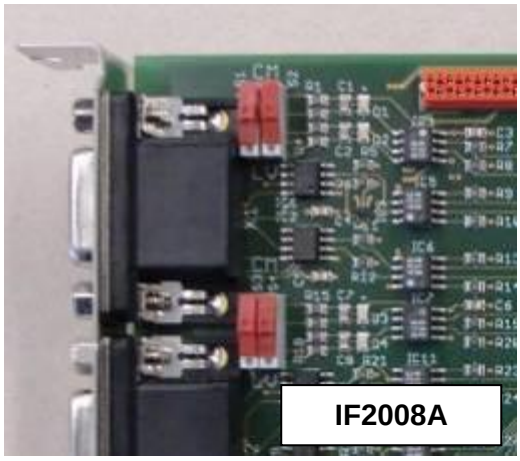


Image 3: Switch settings trigger level

Switch	Setting		Trigger output +
S1 to S6	CMn		3.3 V CMOS level for sensor n TRG+
	LVn		LVDS level for sensor n TRG+

Table 6: Switch settings trigger level

3.7 Switch Settings for ADC Level

By means of the switches S11 to S15 and S21 to S25 the input voltage range of the analogue-digital converter for the sensor channel 5 and 6 on the IF2008E can be selected.

Image 4: Switch settings ADC level

(Settling in the image ±10)

VIN	Sx1	Sx2	Sx3	Sx4	Sx5
0-5 V	ON	ON		ON	ON
0-10 V	ON		ON	ON	ON
±5 V	ON		ON		ON
±10 V		ON	ON		

Table 7: Switch settings ADC level

Setting	
ON	
OFF	

4 Address Assignment

4.1 PCI Interface

Interface: 16 bit PCI bus with 3.3 or 5 Volt connection
Access: Memory space 40 Hex addresses
Base address: Automatic allocation by operating system

Header Configuration

Addr.	Byte 3	Byte 2	Byte 1	Byte 0	Value (Hex)
00h	Device ID		Vendor ID		9030 10B5
18h	Base address local memory space				xxxx xxxx
2C	Subsystem ID		Subsystem Vendor ID		2302 2810

Table 8: Header configuration

4.2 Local Address Assignment

Base addr. +	Write Access	Read Access
00h	Transmit register	FIFO data
02h	Set / reset / latch register	FIFO volume
04h	FIFO enable register	FIFO Enable register
06h	Interrupt enable register	Interrupt state register
08h	Sensor 1 baud rate	remarked
0Ah	Sensor 2 baud rate	remarked
0Ch	Sensor 3 baud rate	remarked
0Eh	Sensor 4 baud rate	remarked
10h	Sensor 5 baud rate	remarked
12h	Sensor 6 baud rate	remarked
14h	Counter control register 1	Counter control register 1
16h	Counter control register 2	Counter control register 2
18h	Counter 1 preload LSW	Counter 1 LSW
1Ah	Counter 1 preload MSW	Counter 1 MSW
1Ch	Counter 2 preload LSW	Counter 2 LSW
1Eh	Counter 2 preload MSW	Counter 2 MSW
20h	Timer 1 frequency	ADC 1
22h	Timer 1 pulse width	ADC 2
24h	Timer 2 frequency	State
26h	Timer 2 pulse width	Input
28h	Timer 3 frequency	remarked
2Ah	Timer 3 pulse width	remarked
2Ch	Timer Clock divider	Timer Clock divider
2Eh	Output register	Output register
30h	Mode opto- and TxD outputs	Mode opto- and TxD outputs
32h	Mode trigger outputs	Mode trigger outputs
34h	ADC control register	ADC control register
36h	Parity enable register	Parity error

Table 9: Local address assignment

5 Register Description

5.1 Transmit Register

The sending register sends commands to the sensor.

Base addr. + 00h (write access)

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
			S6	S5	S4	S3	S2	S1	D7	D6	D5	D4	D3	D2	D1	D0
	Selection sensor channel								Data bits							

Table 10: Transmit register

Bit 0 to 7 Include the data for sending register
Bit 8 to 15 Selection sensor channel

Bit 8 = 1 ➔ Data are output on the sensor channel S1
Bit 9 = 1 ➔ Data are output on the sensor channel S2
etc.
Bit 13 = 1 ➔ Data are output on the sensor channel S6
Bit 14..15 ➔ free

Immediately on the write access to the address “0”, the data with the bit 8 to 13 selected sensor channel are transmitted. The baud rate for the transmit register is automatically adapted to the selected sensor channel. In case that the data output is effected on more channels, the baud rate of the best channel is used.

5.2 FIFO Data

Answering of the sensor, e.g. measuring values are stored in the FIFO memory and are forwarded to the operator by the functions MEDAQLib.

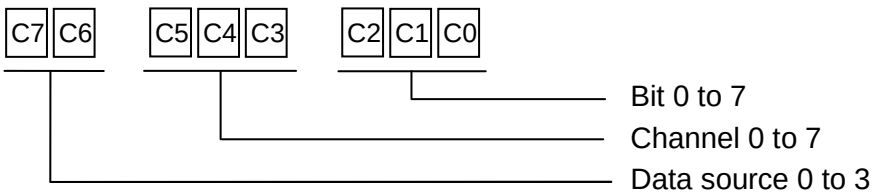
Base addr. + 00h (read access)

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	C7	C6	C5	C4	C3	C2	C1	C0	D7	D6	D5	D4	D3	D2	D1	D0
	Code bits								Data bits							

Table 11: FIFO Data memory

Bit 0 to 7 Include the data buffered
Bit 8 to 15 Mark the data code

Code bits



C7	C6	Data Source
0	0	Sensor
0	1	Encoder
1	0	Switching input (IN 1..4 → channel 0, RxD 1..6 → channel 1)
1	1	ADC

Table 12: FIFO Data memory – Data sources

5.3 Set- / Reset- / Latch Register

Register to affect the counter.
Base addr. + 02h (write access)

Bit	Function
0	Counter 1 delete, i.e. zeroing with //“Clear_Encoder“
1	Counter 1 load, pre-assigned by a value via //“SetEncoderPreload“ forwarded to the IF2008 via //“Load_Encoder“.
2	Counter 1 latch, get current numeric value
3	Counter 1 reference with //“EnableRef_Encoder“, requires Set_EncoderMode
4	Counter 2 delete
5	Counter 2 load
6	Counter 2 latch
7	Counter 2 reference
8	ADC 1 conversion start, //“Get_ADCValue“ converts and gets a value
9	ADC 1 conversion start
10	FIFO delete with //“Clear_Buffers“.
11 – 15	remarked

Table 13: Set- / reset- / latch register

Please note:

- By means of the bits 0 to 2 and 4 to 6 the counters can be either deleted or loaded independently of the counter control register by the software, (addr. 14h and addr. 16h) Furthermore, the counter reading can be transferred into the latch register.
- If a counter latch or load function, which should only operate in connection with a reference marker signal is settled by the counter control register (addr. 14h and addr. 16h); this is subject to approval by setting bit 3 or bit 7. On setting bit 3 or bit 7 the state bits 0 and 1 or 2 and 3 are reset.
- All bits have to be settled, resetting is not necessary
- In case of power failure all bits are set to "0".
- //“ “ Description of the corresponding commands in the MEDAQLib.

5.4 FIFO Volume

Base addr. + 02h (read access)

Bit	Function
0 to 11	FIFO data volume (0 to 4095)
12 to 15	permanent 0

Table 14: FIFO volume

The dataset is transferred automatically into the FIFO data memory on receipt. By means of a report of the FIFO volume the FIFO data amount can be calculated. The order and speed regarding buffering the data received, is similar to the data stream of the receiving register. In case that the FIFO is not readout quickly enough the latest data (4096) received is available.

Is used by the MEDAQLib internally, there is no individual command.

5.5 FIFO Enable Register

The FIFO-Enable-Register is internally dealt by MEDAQLib.

Base addr. + 04h (write and read access)

Bit	Function
0	0 = FIFO for sensor channel 1 blocked 1 = FIFO for sensor channel 1 released
1	0 = FIFO for sensor channel 2 blocked 1 = FIFO for sensor channel 2 released
2	0 = FIFO for sensor channel 3 blocked 1 = FIFO for sensor channel 3 released
3	0 = FIFO for sensor channel 4 blocked 1 = FIFO for sensor channel 4 released
4	0 = FIFO for sensor channel 5 blocked 1 = FIFO for sensor channel 5 released
5	0 = FIFO for sensor channel 6 blocked 1 = FIFO for sensor channel 6 released
6	0 = FIFO for encoder channel 1 blocked 1 = FIFO for encoder channel 1 released
7	0 = FIFO for encoder channel 2 blocked 1 = FIFO for encoder channel 2 released
8	0 = FIFO for state of external inputs IN 1..4 blocked 1 = FIFO for state of external inputs IN 1..4 released
9	0 = FIFO for state of RxD inputs (sensor 1..6) blocked 1 = FIFO for state of RxD inputs (sensor 1..6) released
10	0 = FIFO for ADC 1 blocked 1 = FIFO for ADC 1 released
11	0 = FIFO for ADC 2 blocked 1 = FIFO for ADC 2 released
12	0 = FIFO in case of active, ext. Input IN 1 for sensor 1 and 2 blocked 1 = IN 1 has no affect on FIFO
13	0 = FIFO in case of active, ext. Input IN 2 for sensor 3 and 6 blocked 1 = IN 2 has no affect on FIFO
14	0 = FIFO in case of active, ext. Input IN 3 for encoder 1 and 2 blocked 1 = IN 3 has no affect on FIFO
15	0 = FIFO in case of active, ext. Input IN 4 for ADC ½; IN 1..4; RxD 1..6 blocked 1 = IN 4 has no affect on FIFO

Table 15: FIFO enable register

Data acquisition in blocks. Defines which data e.g. of the sensors will be stored in the FIFO. The FIFO has 4095 bytes. If 2/3 of the capacity in the FIFO are reached, the driver of the IF card evaluates the data of the FIFO and stores them in the driver buffer at a maximum rate of 64kByte. The MEDAQLib gets the data from the driver buffer and stores them in the ring buffer at a maximum rate of 10MByte. Note for bit 9: The RxD inputs can also be used as further control inputs, e.g. of a SPS in the case that the external inputs are not sufficient.

Note for bit 12 to 15: Therefore, the measuring values can either be blocked or evaluated (gating). The command in the MEDAQLib is Use_Gate.

5.6 Interrupt Enable Register

Base addr. + 06h (write access)

Bit	Function
0	1 = Enable interrupt requirements if FIFO more than 50 % reserved
1	1 = Enable interrupt requirements if FIFO more than 75% reserved
2	1 = Enable interrupt requirements on overflow Timer 1
3	1 = Enable interrupt requirements on overflow Timer 2
4	1 = Enable interrupt requirements on overflow Timer 3
5	1 = Enable interrupt requirements if external input IN 1 is activated
6	1 = Enable interrupt requirements if external input IN 2 is activated
7	1 = Enable interrupt requirements if external input IN 3 is activated
8	1 = Enable interrupt requirements if external input IN 4 is activated
9 - 15	remarked

Table 16: Interrupt enable register

The MEDAQLib uses bit 1, more than 75 % of the FIFO is used. The interrupt function enables the data evaluation in the driver buffer.

Please note:

The interrupt generation is controlled by a trigger flange, that means an interrupt requirement is only effected if the corresponding bit is set in the interrupt enable register. Furthermore, the appropriate source has to change from the inactive into the active state. More than one bit can be set at the same time.

5.7 Interrupt State Register

Base addr. + 06h (read access)

Bit	Function
0	1 = Interrupt requirement in case of FIFO level more than 50 %
1	1 = Interrupt requirement in case of FIFO level more than 75 %
2	1 = Interrupt requirement on overflow Timer 1
3	1 = Interrupt requirement on overflow Timer 2
4	1 = Interrupt requirement on overflow Timer 3
5	1 = Interrupt requirements on activating the external input IN 1
6	1 = Interrupt requirements on activating the external input IN 2
7	1 = Interrupt requirements on activating the external input IN 3
8	1 = Interrupt requirements on activating the external input IN 4
9 - 15	remarked

Table 17: Interrupt status register

Enables a report which interrupt has occured. The MEDAQLib uses bit 1. The register can not be reached from outside, it is only used by the driver.

Please note:

The interrupt state register informs by which source(s) the interrupt requirements have been generated. One interrupt requirement can be effected by using more than one source at the same time. In case that no state bit is set, the interrupt requirement was not generated by the IF2008A but by another hardware.

5.8 Sensor Baud Rate

Base addr.	Sensor Channel	Value	Access
+ 08h	1	1 to 65,535	write access only
+ 0Ah	2	1 to 65,535	write access only
+ 0Ch	3	1 to 65,535	write access only
+ 0Eh	4	1 to 65,535	write access only
+ 10h	5	1 to 65,535	write access only
+ 12h	6	1 to 65,535	write access only

Table 18: Base addresses for sensor baud rates

Depending on the sensor, the register is set automatically. It cannot be reached directly by the operator. In the case of sensors with a variable baud rate, the baud rate can be set while opening the sensor. Additionally, the MEDAQLib sets the corresponding baud rate in the IF card.

Value = (40 MHz / Baud rate) - 1

Example:

Requested baud rate = 691.2 kBaud

Value = (40 MHZ / 691.200) - 1 = 56.87

The input value has to be an integer i.e. the result has to be rounded:

➔ **Value = 57**

5.9 Counter Controll Register

Base Adr	Counter Channel	Bit	Access
+ 14h	1	0 to 15	write and read access
+ 16h	2	0 to 15	write and read access

Table 19: Base addresses for counter control register

The counter control register states the operating procedure of the encoder.
The tabels below are similar to both counter channels!

Functional Overview

Bit	Function
0 to 3	Interpolation (see Table 21: Encoder interpolation) //Set_EncoderInterpolation respectively Get_EncoderInterpolation
4	Direction of counting (see Table 22: Encoder counter direction) //Set_EncoderDirection respectively Get_EncoderDirection
5 to 7	Counter mode (see table 23: counter mode) //Set_EncoderMode respectively Get_EncoderMode
8 to 11	Latch source (see table 24: counter latch source) //Set_EncoderLatchSource respectively Get_EncoderLatchSource
12 to 15	remarked

Table 20: Functional overview for counter control register

Interpolation

Bit 3	Bit 2	Bit 1	Bit 0	Interpolation
0	0	0	0	1
0	0	0	1	2
0	0	1	0	3
0	0	1	1	4
0	1	0	0	5
0	1	0	1	6
0	1	1	0	8
0	1	1	1	10
1	0	0	0	12
1	0	0	1	16
1	0	1	0	20
1	0	1	1	24
1	1	0	0	32
1	1	0	1	40
1	1	1	0	48
1	1	1	1	64

Table 21: Encoder interpolation

Please note:
- for encoders with 1 V_{ss} – signals all interpolations are suitable
- for encoders with TTL – signals the following interpolations are suitable: 1-, 2- or 4-times. For example 4 times interpolation: In the case of an increasing or falling flank and track A and track B, therefore 4 times of counting pulses.

Counter Direction

Bit 4	Counter Direction
0	usual
1	inverse

Table 22: Encoder counter direction

Counter Mode:

The counter mode sets the operating procedure of the encoder in the case of references.

<table>
<tr><th>Bit 7</th><th>Bit 6</th><th>Bit 5</th><th>Counter Mode</th></tr>
<tr><td>0</td><td>0</td><td>0</td><td>No counter load or delete function by encoder reference marker</td></tr>
<tr><td>0</td><td>0</td><td>1</td><td>Counter is loaded with the next encoder reference marker as far as the state bit 0 or state bit 2 “0” is settled.</td></tr>
<tr><td>0</td><td>1</td><td>0</td><td>Counter is loaded including all encoder reference markers and load register content. State bit 0 to 3 are not affected.</td></tr>
<tr><td>0</td><td>1</td><td>1</td><td>Counter is deleted including all encoder reference markers and additionally loaded with the content of the load register if the counter has reached -1. This function offers the possibility to limit the counter. During this process the counter load register has to be preallocated with the number of increments limited -1.</td></tr>
<tr><td>1</td><td>0</td><td>0</td><td>Counter exluded phase discriminator (Counter)
<table>
<tr><th>Bit 4</th><th>Function</th></tr>
<tr><td rowspan="2">0</td><td>Track A = counter direction signal</td></tr>
<tr><td>Track B = counter clock signal</td></tr>
<tr><td rowspan="2">1</td><td>Track A = counter clock signal</td></tr>
<tr><td>Track B = counter direction signal</td></tr>
</table></td></tr>
<tr><td>1</td><td>0</td><td>1</td><td>remarked</td></tr>
</table>

1	1	0	remarked
1	1	1	remarked

Table 23: Counter

Latch Source:

Enables the synchronised acquisition of the sensor and the encoder values. The command in the MEDAQLib is Set_EncoderLatchSource.

Bit 11	Bit 10	Bit 9	Bit 8	Latch Source
0	0	0	0	Hardware latch blocked
0	0	0	1	Timer 1
0	0	1	0	Timer 2
0	0	1	1	Timer 3
0	1	0	0	Sensor channel 1
0	1	0	1	Sensor channel 2
0	1	1	0	Sensor channel 3
0	1	1	1	Sensor channel 4
1	0	0	0	Sensor channel 5
1	0	0	1	Sensor channel 6
1	0	1	0	IN 1 (IF2008E only)
1	0	1	1	IN 2 (IF2008E only)
1	1	0	0	IN 3 (IF2008E only)
1	1	0	1	IN 4 (IF2008E only)
1	1	1	0	2. reference
1	1	1	1	All reference markers

Table 24: Counter latch source

5.10 Counter Preload

Pre-Assignment register for the encoder starting values, 32 bit wide. The command in the MEDAQLib is Set_EncoderPreload.

Base addr.	Counter Channel	Value	Access
+ 18h	1 LSW	0 to 65,535	Write access only
+ 1Ah	1 MSW	0 to 65,535	Write access only
+ 1Ch	2 LSW	0 to 65,535	Write access only
+ 1Eh	2 MSW	0 to 65,535	Write access only

Table 25: Base addresses for counter preload

5.11 Counter Value

Command for evaluation. The command in the MEDAQLib is Get_EncoderValue.

Base addr.	Counter Channel	Value	Access
+ 18h	1 LSW	0 to 65,535	Read access only
+ 1Ah	1 MSW	0 to 65,535	Read access only
+ 1Ch	2 LSW	0 to 65,535	Read access only
+ 1Eh	2 MSW	0 to 65,535	Read access only

Table 26: Base addresses for counter value

LSW = Least significant word

MSW = Most significant word

5.12 Timer

Command in the MEDAQLib: Set_TimerFrequency.
Application:

- Set Timer to digital output
- Synchronising data acquisition
- Get triggering signal

Example: Time-based synchronising of the sensor using the command Set_TriggerSource.

Base addr.	Timer	Value	Access:
+ 20h	1 frequency	0 to 65,535	Write access only
+ 22h	1 pulse width	0 to 65,535	Write access only
+ 24h	2 frequency	0 to 65,535	Write access only
+ 26h	2 pulse width	0 to 65,535	Write access only
+ 28h	3 frequency	0 to 65,535	Write access only
+ 2Ah	3 pulse width	0 to 65,535	Write access only
+ 2Ch	Clock divider		Write and read access

Table 27: Base addresses for timer

$$\mathbf{Value(F) = (F_{Clock} / F_{OUT}) - 1}$$
$$\mathbf{Value(PW) = (PW_{OUT} / T_{Clock})}$$

Example:

Requested frequency F_{OUT} = 10 kHz

Requested pulse width PW_{OUT} = 25 µs

Clock divider = 0 → F_{Clock} = 20 MHZ, T_{Clock} = 50 ns (clock divider see table below)

Value(F) = (20 MHZ / 10 kHz) - 1 = 1999

Value(PW) = (25 µs / 50 ns) = 500

The input values have to be integer!

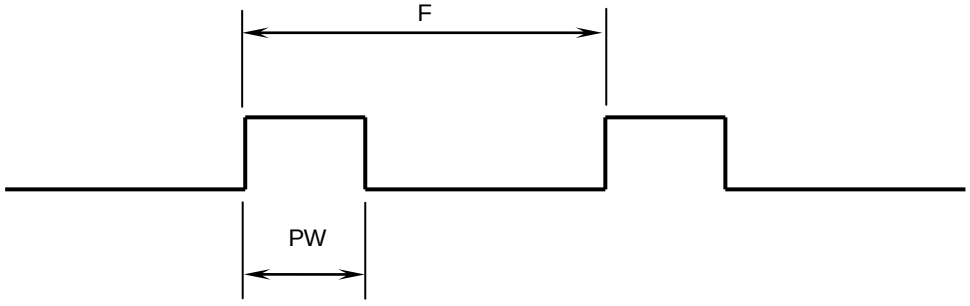


Image 5: Timer frequency and pulse width

Please note:

The pulse width only affects the output “sensor trigger” and “optocoupler”.

The internal synchronization signals are not affected. The timer zero crossing is used.

In order to switch off the timer, the frequency "0" has to be set. If in case of an inactive timer the pulse width is set > 0, the output is permanently set on high. On the contrary, if the pulse width is set “0”, the output is permanently set on low.

Clock Divider:

Bit 3	Bit 2	Bit 1	Bit 0	Clock Frequency Timer 1
Bit 7	**Bit 6**	**Bit 5**	**Bit 4**	**Clock Frequency Timer 2**
Bit 11	**Bit 10**	**Bit 9**	**Bit 8**	**Clock Frequency Timer 3**
0	0	0	0	20 MHz
0	0	0	1	20 MHz / 2
0	0	1	0	20 MHz / 4
0	0	1	1	20 MHz / 8
0	1	0	0	20 MHz / 16
0	1	0	1	20 MHz / 32
0	1	1	0	20 MHz / 64
0	1	1	1	20 MHz / 128
1	0	0	0	20 MHz / 256
1	0	0	1	20 MHz / 512
1	0	1	0	20 MHz / 1024
1	0	1	1	20 MHz / 2048
1	1	0	0	20 MHz / 4096
1	1	0	1	20 MHz / 8192
1	1	1	0	20 MHz / 16384
1	1	1	1	20 MHz / 32768

Table 28: Timer clock divider

Please note:

Bit 12 to bit 15 are remarked.

5.13 ADC

Two register for the currently converted values of the A/D converter. MEDAQLib evaluates the values using the command Get_ADCValue or by storing them in the FIFO.

Base addr.	ADC Channel	Value	Access
+ 20h	1	0 to 65535	Read access only
+ 22h	2	0 to 65535	Read access only

Table 29: Base addresses for ADC

5.14 State

Base addr. + 24h (read access only)

Bit	Function
0	1 = Encoder 1: 1. reference markers crossed //Get_EncoderReference
1	1 = Encoder 1: 2. reference markers crossed
2	1 = Encoder 2: 1. reference markers crossed
3	1 = Encoder 2: 2. reference markers crossed
4	0 = Transmitter ready for new data transfer 1 = Transmitter is occupied
5	0 = no extension module with sensor 5 / 6 available 1 = no extension module with sensor 5 / 6 available
6	0 = no extension module for external I/O available 1 = no extension module for external I/O available
7	0 = no extension module with ADC available 1 = no extension module with ADC available
8 – 15	Version FPGA

Table 30: State

Note for bit 4: Internal use. The IF card requires more time for sending commands to the sensor than the MEDAQLib to the IF card. With this bit the MEDAQLib checks if the IF card is ready for further applications.

Note for bit 5, 6, 7: Internal use. Displays if the IF2008E is connected. Commands for querying the bits: Is_Channel56Available, Is_ADCAvailable or IS_DigitalOAvailable.

5.15 Input

Base addr. + 26h (read access only)

Bit	Function
0	1 = ext. Input IN 1 active
1	1 = ext. Input IN 2 active
2	1 = ext. Input IN 3 active
3	1 = ext. Input IN 4 active
4	1 = RxD input on the sensor input 1 active
5	1 = RxD input on the sensor input 2 active
6	1 = RxD input on the sensor input 3 active
7	1 = RxD input on the sensor input 4 active
8	1 = RxD input on the sensor input 5 active
9	1 = RxD input on the sensor input 6 active
8 – 15	remarked

Table 31: Input

Note for bit 0 to 3: Internal use. Displays if the digital inputs are High or Low Command: Get_DigitalInValue.

Note for bit 4 to 9: Internal use. Displays if the RxD inputs are High or Low Command: Get_RxDValue.

5.16 Output Register

Base addr. + 2Eh (write and read access)

Bit	Function			Output Signal
0	0 = OUT 1 OFF 1 = OUT 1 ON	Optocoupler blocked Optocoupler conductive	[1]	Output 1 = High Output 1 = Low //Set_DigitalOutValue respect. Get_DigitalOutValue
1	0 = OUT 2 OFF 1 = OUT 2 ON	Optocoupler blocked Optocoupler conductive	[1]	Output 2 = High Output 2 = Low
2	0 = OUT 3 OFF 1 = OUT 3 ON	Optocoupler blocked Optocoupler conductive	[1]	Output 3 = High Output 3 = Low
3	0 = OUT 4 OFF 1 = OUT 4 ON	Optocoupler blocked Optocoupler conductive	[1]	Output 4 = High Output 4 = Low
4	0 = TxD 1 1 = TxD 1	inactive active		TxD 1+ = High TxD 1- = Low TxD 1+ = Low TxD 1- = High //Set_TxDValue respect. Get_TxDValue
5	0 = TxD 2 1 = TxD 2	inactive active		TxD 2+ = High TxD 2- = Low TxD 2+ = Low TxD 2- = High
6	0 = TxD 3 1 = TxD 3	inactive active		TxD 3+ = High TxD 3- = Low TxD 3+ = Low TxD 3- = High
7	0 = TxD 4 1 = TxD 4	inactive active		TxD 4+ = High TxD 4- = Low TxD 4+ = Low TxD 4- = High
8	0 = TxD 5 1 = TxD 5	inactive active	[1]	TxD 5+ = High TxD 5- = Low TxD 5+ = Low TxD 5- = High
9	0 = TxD 6 1 = TxD 6	inactive active	[1]	TxD 6+ = High TxD 6- = Low TxD 6+ = Low TxD 6- = High
10	0 = TRG 1 1 = TRG 1	inactive active		TRG 1+ = Low TRG 1- = High TRG 1+ = High TRG 1- = Low //Set_TrgValue respect. Get_TrgValue
11	0 = TRG 2 1 = TRG 2	inactive active		TRG 2+ = Low TRG 2- = High TRG 2+ = High TRG 2- = Low
12	0 = TRG 3 1 = TRG 3	inactive active		TRG 3+ = Low TRG 3- = High TRG 3+ = High TRG 3- = Low
13	0 = TRG 4 1 = TRG 4	inactive active		TRG 4+ = Low TRG 4- = High TRG 4+ = High TRG 4- = Low
14	0 = TRG 5 1 = TRG 1	inactive active	[1]	TRG 5+ = Low TRG 5- = High TRG 5+ = High TRG 5- = Low
15	0 = TRG 6 1 = TRG 6	inactive active	[1]	TRG 6+ = Low TRG 6- = High TRG 6+ = High TRG 6- = Low

Table 32: Output register

Please note:

For all outputs more signal sources are available. Bits listed above are only connected trough in case that the appropriate mode is set (see table 33 on page 22: mode opto- and TxD outputs).

[1] Expansion Board only

5.17 Mode Opto- and TxD Outputs

Base addr. + 30h (write and read access)

<table>
<tr><th>Bit</th><th>Function</th></tr>
<tr><td>0 and 1</td><td>
<table>
<tr><th>Bit 1</th><th>Bit 0</th><th>Function</th></tr>
<tr><td>0</td><td>0</td><td>Output 1 connects with addr. 2Eh bit 0
//Set_DigitalOutSource respectively Get_DigitalOutSource</td></tr>
<tr><td>0</td><td>1</td><td>Output 1 connects with timer 1 pulse width</td></tr>
<tr><td>1</td><td>0</td><td>Output 1 connects with timer 2 pulse width</td></tr>
<tr><td>1</td><td>1</td><td>Output 1 connects with timer 3 pulse width</td></tr>
</table>
</td></tr>
<tr><td>2 and 3</td><td>
<table>
<tr><th>Bit 3</th><th>Bit 2</th><th>Function</th></tr>
<tr><td>0</td><td>0</td><td>Output 2 connects with addr. 2Eh bit 1</td></tr>
<tr><td>0</td><td>1</td><td>Output 2 connects with timer 1 pulse width</td></tr>
<tr><td>1</td><td>0</td><td>Output 2 connects with timer 2 pulse width</td></tr>
<tr><td>1</td><td>1</td><td>Output 2 connects with timer 3 pulse width</td></tr>
</table>
</td></tr>
<tr><td>4 and 5</td><td>
<table>
<tr><th>Bit 5</th><th>Bit 4</th><th>Function</th></tr>
<tr><td>0</td><td>0</td><td>Output 3 connects with addr. 2Eh bit 2</td></tr>
<tr><td>0</td><td>1</td><td>Output 3 connects with timer 1 pulse width</td></tr>
<tr><td>1</td><td>0</td><td>Output 3 connects with timer 2 pulse width</td></tr>
<tr><td>1</td><td>1</td><td>Output 3 connects with timer 3 pulse width</td></tr>
</table>
</td></tr>
<tr><td>6 and 7</td><td>
<table>
<tr><th>Bit 7</th><th>Bit 6</th><th>Function</th></tr>
<tr><td>0</td><td>0</td><td>Output 4 connects with addr. 2Eh bit 3</td></tr>
<tr><td>0</td><td>1</td><td>Output 4 connects with timer 1 pulse width</td></tr>
<tr><td>1</td><td>0</td><td>Output 4 connects with timer 2 pulse width</td></tr>
<tr><td>1</td><td>1</td><td>Output 4 connects with timer 3 pulse width</td></tr>
</table>
</td></tr>
<tr><td>8</td><td>0 = TxD 1 connects with transmitter
1 = TxD 1 connects with addr. 2Eh bit 4
//Set_TxDSource respectively Get_TxDSource</td></tr>
<tr><td>9</td><td>0 = TxD 2 connects with transmitter
1 = TxD 2 connects with addr. 2Eh bit 5</td></tr>
<tr><td>10</td><td>0 = TxD 3 connects with transmitter
1 = TxD 3 connects with addr. 2Eh bit 6</td></tr>
<tr><td>11</td><td>0 = TxD 4 connects with transmitter
1 = TxD 4 connects with addr. 2Eh bit 7</td></tr>
<tr><td>12</td><td>0 = TxD 5 connects with transmitter
1 = TxD 5 connects with addr. 2Eh bit 8</td></tr>
<tr><td>13</td><td>0 = TxD 6 connects with transmitter
1 = TxD 6 connects with addr. 2Eh bit 9</td></tr>
<tr><td>14 - 15</td><td>remarked</td></tr>
</table>

Table 33: Mode Opto- and TxD Outputs

Please note:

The outputs 1 to 4 are only available for the IF2008E.

5.18 Mode Trigger Outputs

Base addr. + 32h (write and read access)
Configures the six trigger outputs, command in the MEDAQLib is Set_TrgSource.

Bit	Function

0 and 1

Bit 1	Bit 0	Function
0	0	Trigger 1 connects with addr. 2Eh bit 10
0	1	Trigger 1 connects with timer 1 pulse width
1	0	Trigger 1 connects with timer 2 pulse width
1	1	Trigger 1 connects with timer 3 pulse width

2 and 3

Bit 3	Bit 2	Function
0	0	Trigger 2 connects with addr. 2Eh bit 11
0	1	Trigger 2 connects with timer 1 pulse width
1	0	Trigger 2 connects with timer 2 pulse width
1	1	Trigger 2 connects with timer 3 pulse width

4 and 5

Bit 5	Bit 4	Function
0	0	Trigger 3 connects with addr. 2Eh bit 12
0	1	Trigger 3 connects with timer 1 pulse width
1	0	Trigger 3 connects with timer 2 pulse width
1	1	Trigger 3 connects with timer 3 pulse width

6 and 7

Bit 7	Bit 6	Function
0	0	Trigger 4 connects with addr. 2Eh bit 13
0	1	Trigger 4 connects with timer 1 pulse width
1	0	Trigger 4 connects with timer 2 pulse width
1	1	Trigger 4 connects with timer 3 pulse width

8 and 9

Bit 9	Bit 8	Function
0	0	Trigger 5 connects with addr. 2Eh bit 14
0	1	Trigger 5 connects with timer 1 pulse width
1	0	Trigger 5 connects with timer 2 pulse width
1	1	Trigger 5 connects with timer 3 pulse width

10 and 11

Bit 11	Bit 10	Function
0	0	Trigger 6 connects with addr. 2Eh bit 15
0	1	Trigger 6 connects with timer 1 pulse width
1	0	Trigger 6 connects with timer 2 pulse width
1	1	Trigger 6 connects with timer 3 pulse width

<table>
<tr><th>Bit</th><th>Function</th></tr>
<tr><td>12 – 14</td><td>
<table>
<tr><th>Bit 14</th><th>Bit 13</th><th>Bit 12</th><th>Latch Source</th></tr>
<tr><td>0</td><td>0</td><td>0</td><td>Hardware latch blocked</td></tr>
<tr><td>0</td><td>0</td><td>1</td><td>Timer 1</td></tr>
<tr><td>0</td><td>1</td><td>0</td><td>Timer 2</td></tr>
<tr><td>0</td><td>1</td><td>1</td><td>Timer 3</td></tr>
<tr><td>1</td><td>0</td><td>0</td><td>Sensor channel 1</td></tr>
<tr><td>1</td><td>0</td><td>1</td><td>Sensor channel 2</td></tr>
<tr><td>1</td><td>1</td><td>0</td><td>Sensor channel 3</td></tr>
<tr><td>1</td><td>1</td><td>1</td><td>Sensor channel 4</td></tr>
</table>
</td></tr>
<tr><td>15</td><td>remarked</td></tr>
</table>

Table 34: Mode trigger outputs

Please note:

By means of bits 12-14 a latch source can be selected. The trigger process of the external inputs (IN1-4) and RxD input (sensor 1-6) allows recording the results synchronously to the FIFO.

The command in the MEDAQLib is Set_DigitalLatchSource.

5.19 ADC Control Register

Defining bit 0 to 7, when acquiring and evaluating an AD value in the FIFO. The synchronisation can be effected using a timer, a sensor cable or an pulse on the digital input IN1 … IN4. Therefore an external triggering is possible due to the digital inputs.
Base addr. + 34h (write and read access)

Bit 3	Bit 2	Bit 1	Bit 0	Conversion Source ADC1
Bit 7	**Bit 6**	**Bit 5**	**Bit 4**	**Conversion Source ADC2**
0	0	0	0	Hardware converter blocked
0	0	0	1	Timer 1
0	0	1	0	Timer 2
0	0	1	1	Timer 3
0	1	0	0	Sensor channel 1
0	1	0	1	Sensor channel 2
0	1	1	0	Sensor channel 3
0	1	1	1	Sensor channel 4
1	0	0	0	Sensor channel 5
1	0	0	1	Sensor channel 6
1	0	1	0	IN 1 (IF2008E/ I/O only)
1	0	1	1	IN 2 (IF2008E/ I/O only)
1	1	0	0	IN 3 (IF2008E/ I/O only)
1	1	0	1	IN 4 (IF2008E/ I/O only)
1	1	1	0	remarked
1	1	1	1	remarked

Table 35: ADC control register bit 0-7

Bit	Function
8	0 = ADC1 data output binary 2-complement 1 = ADC 1 data output binary not converted
9	0 = ADC2 data output binary 2-complement 1 = ADC2 data output binary not converted
10 – 15	remarked

Table 36: ADC control register bit 8-15

Note for bit 8 and 9: Internal use. Function is not used in the MEDAQLib. The MEDAQLib cannot evaluate the switch setting for the analogue sections.

Analog Input				Digital Output	
0 – 5 V	0 – 10 V	+/-5 V	+/-10 V	Binary 2-complement	Binary not converted
+4.99 V	+9.99 V	+4.99 V	+9.99 V	7FFF	FFFF
2.5 V	5 V	0 V	0 V	0000	8000
+2.499 V	+4.999 V	-153 µV	-305 µV	FFFF	7FFF
0 V	0 V	-5 V	-10 V	8000	0000

Table 37: ADC converting result

5.20 Parity Enable Register

Base addr. + 36 0(write access)

Bit	Function
0	0 = Parity bit for sensor channel 1 blocked 1 = Parity bit for sensor channel 1 released (even parity only)
1	0 = Parity bit for sensor channel 2 blocked 1 = Parity bit for sensor channel 2 released (even parity only)
2	0 = Parity bit for sensor channel 3 blocked 1 = Parity bit for sensor channel 3 released (even parity only)
3	0 = Parity bit for sensor channel 4 blocked 1 = Parity bit for sensor channel 4 released (even parity only)
4	0 = Parity bit for sensor channel 5 blocked 1 = Parity bit for sensor channel 5 released (even parity only)
5	0 = Parity bit for sensor channel 6 blocked 1 = Parity bit for sensor channel 6 released (even parity only)
6-15	remarked

Table 38: Parity enable register

In the case that a sensor e.g. a time-of-flight sensor which data protocol uses the parity bit is chosen, the MEDAQLib activates the corresponding parity register automatically.

5.21 Parity Error Register

Base addr. + 36h (read access)

Bit	Function
0	1 = parity error sensor channel 1
1	1 = parity error sensor channel 2
2	1 = parity error sensor channel 3
3	1 = parity error sensor channel 4
4	1 = parity error sensor channel 5
5	1 = parity error sensor channel 6
6 – 15	remarked

Table 39: Parity error register

6 Recommendation Regarding Cabling

6.1 Sensor ILD1302 and ILD1402

Pin X1/X2 IF2008A Pin X1 IF2008E	Signal	ILD 1302, ILD1402		Signal Sensor
		Pin Sensor 1	Pin Sensor 2	
1	Sensor 1 TxD-	4		RxD-
2	Sensor 1 TxD+	3		RxD+
3	Sensor 1 RxD-	6		TxD-
4	Sensor 1 RxD+	5		TxD+
5	Power supply 0 V	12	12	GND
6	Sensor 1 TRG+	9		TeachIn
7	Sensor 1 TRG-	NC	NC	
8	Sensor 2 TRG+		9	TeachIn
9	Sensor 2 TRG-	NC	NC	
10	Power supply +24 V	7	7	+UB
11	Sensor 2 TxD-		4	RxD-
12	Sensor 2 TxD+		3	RxD+
13	Sensor 2 RxD-		6	TxD-
14	Sensor 2 RxD+		5	TxD+
15	GND (galvanic isolation to PC-GND)	12	12	GND

Table 40: Sensor cabling ILD1302 and ILD1402

6.2 Sensor ILD1700

Pin X1/X2 IF2008A Pin X1 IF2008E	Signal	ILD1700		Signal Sensor
		Pin Sensor 1	Pin Sensor 2	
1	Sensor 1 TxD-	11		RxD-
2	Sensor 1 TxD+	12		RxD+
3	Sensor 1 RxD-	2		TxD-
4	Sensor 1 RxD+	1		TxD+
5	Power supply 0 V	6	6	GND
6	Sensor 1 TRG+	3		TRG+
7	Sensor 1 TRG-	4		TRG-
8	Sensor 2 TRG+		3	TRG+
9	Sensor 2 TRG-		4	TRG-
10	Power supply +24 V	5	5	+UB
11	Sensor 2 TxD-		11	RxD-
12	Sensor 2 TxD+		12	RxD+
13	Sensor 2 RxD-		2	TxD-
14	Sensor 2 RxD+		1	TxD+
15	GND (galvanic isolation to PC-GND)	6	6	GND

Table 41: Sensor cabling ILD1700

6.3 Sensor ILD2200

Pin X1/X2 IF2008A Pin X1 IF2008E	Signal	ILD2200		Signal Sensor
		Pin Sensor 1	Pin Sensor 2	
1	Sensor 1 TxD-	24		RxD-
2	Sensor 1 TxD+	11		RxD+
3	Sensor 1 RxD-	10		TxD-
4	Sensor 1 RxD+	23		TxD+
5	Power supply 0 V	14	14	Supply ground
6	Sensor 1 TRG+	20		SyncIn+
7	Sensor 1 TRG-	NC		
8	Sensor 2 TRG+		20	SyncIn+
9	Sensor 2 TRG-		NC	
10	Power supply +24 V	1	1	+UB
11	Sensor 2 TxD-		24	RxD-
12	Sensor 2 TxD+		11	RxD+
13	Sensor 2 RxD-		10	TxD-
14	Sensor 2 RxD+		23	TxD+
15	GND (galvanic isolation to PC-GND)	7	7	SyncIn-

Table 42: Sensor cabling ILD2200

6.4 Sensor ILD2300

Pin X1/X2 IF2008A Pin X1 IF2008E	Signal	ILD2300		Signal Sensor
		Pin Sensor 1	Pin Sensor 2	
1	Sensor 1 TxD-	8		RxD-
2	Sensor 1 TxD+	7		RxD+
3	Sensor 1 RxD-	10		TxD-
4	Sensor 1 RxD+	9		TxD+
5	Power supply 0 V	2	2	Supply ground
6	Sensor 1 TRG+	5		SyncIn+
7	Sensor 1 TRG-	6		SyncIn-
8	Sensor 2 TRG+		5	SyncIn+
9	Sensor 2 TRG-		6	SyncIn-
10	Power supply +24 V	1	1	+UB
11	Sensor 2 TxD-		8	RxD-
12	Sensor 2 TxD+		7	RxD+
13	Sensor 2 RxD-		10	TxD-
14	Sensor 2 RxD+		9	TxD+
15	GND (galvanically isolated to GND PC)	2	2	

Table 43: Sensor cabling ILD2300

6.5 Encoder Interface

Pin X3 IF2008A	Signal	$1V_{ss}$ or RS422		TTL (single-ended)	
		Signal Encoder 1	Signal Encoder 2	Signal Encoder 1	Signal Encoder 2
1	Encoder 1 track A+	A+		A	
2	Encoder 1 track A-	A-		open	
3	Encoder 2 track A+		A+		A
4	Encoder 2 track A-		A-		open
5	VCC (+5 V)	+UB	+UB	+UB	+UB
6	Encoder 1 track B+	B+		B	
7	Encoder 1 track B-	B-		open	
8	Encoder 2 track B+		B+		B
9	Encoder 2 track B-		B-		open
10	GND	GND	GND	GND	GND
11	Encoder 1 track R+	R+		R	
12	Encoder 1 track R-	R-		open	
13	Encoder 2 track R+		R+		R
14	Encoder 2 track R-		R-		open
15	GND	GND	GND	GND	GND

Table 44: Encoder interface

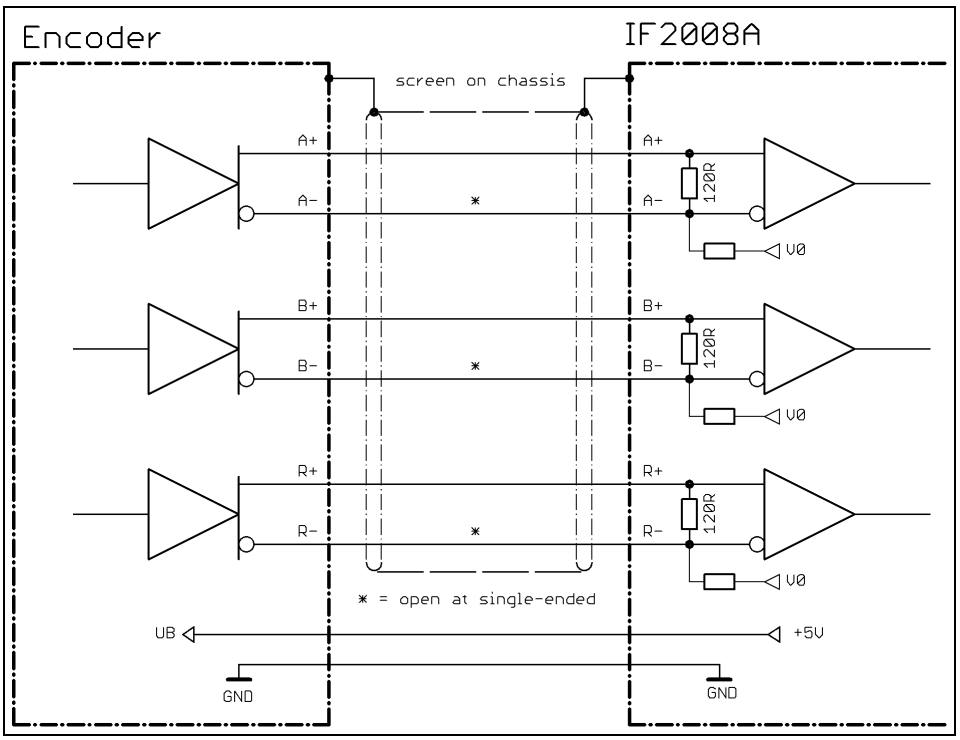


Image 6: Block diagram encoder interface

Please note:
Non-inverting inputs (A+, B+, R+) may not keep open. For example, if only the clock is used regarding the counter, the plus inputs have to be set on GND or VCC.
Not assigned negative inputs (A-, B-, R-) may not be connected with GND.

6.6 Optocoupler I/O

Pin X2 IF2008E	Signal
1	OUT 1
2	OUT 2
3	OUT 3
4	OUT 4
5	GND (galvanic isolation to PC-GND)
6	IN 1
7	IN 2
8	IN 3
9	IN 4

Table 45: Optocoupler I/O

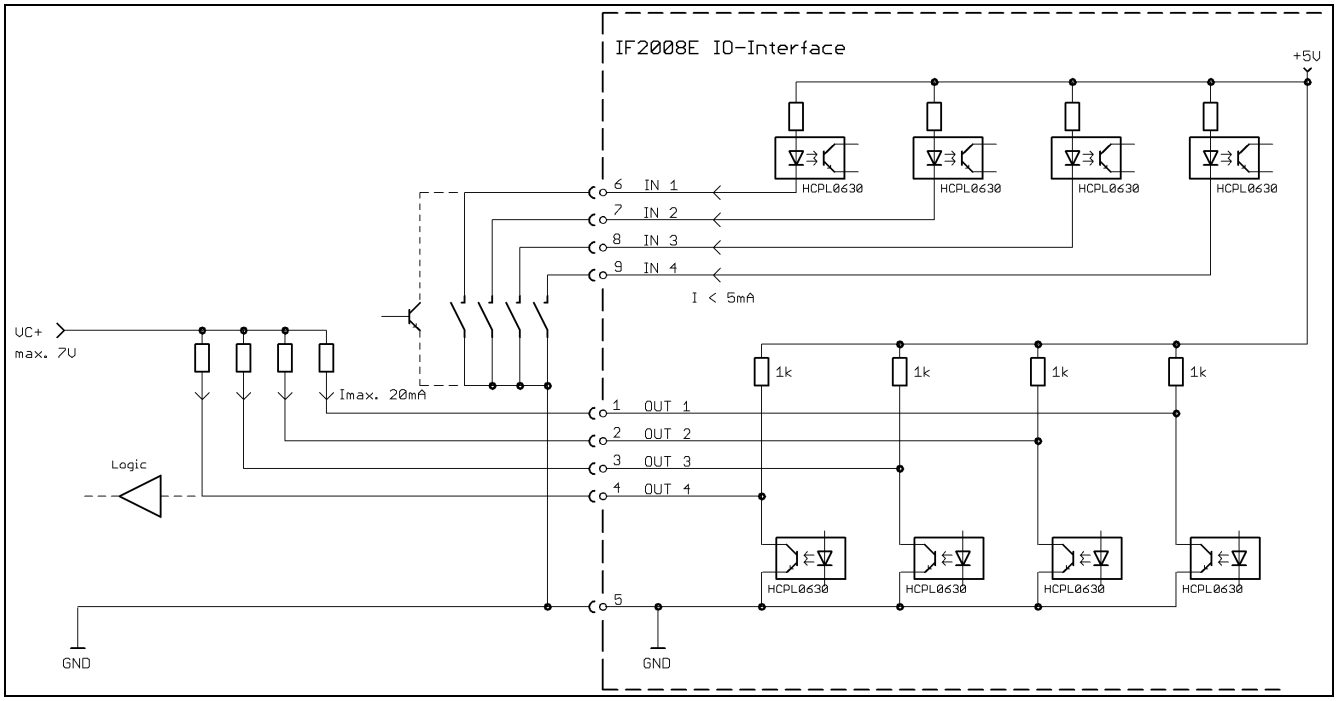


Image 7: Block diagram optocoupler I/O

7 Examples for Synchronisation, Triggering, Gating

Synchronisation = fast application (passive, only „listening“)
Triggering = slow application (active, command and answer)

The following examples show using the ILD1700 sensor as an example the possibilities for data acquisition.

7.1 Get a Measuring Value from the Sensor, Software-trigger

- SET_ERROROUTPUT
- GET_MEASVALUE: One measuring value or more.
- DATAAVAIL: One measuring value or more are available.
- TRANSFERDATA: Evaluates a measuring value from the ring buffer.

7.2 Hardware-Trigger

- SET_ERROROUTPUT: Sensor set in trigger mode, X = “2“ or “3“.
- SET_SYNCMODE/TRIGGERMODE: Set the reaction of the sensor input to the flank or level
- Square pulse on the sensor input caused by e.g. the SPS or trigger output of the IF2008.
- DATAAVAIL: not absolutely necessary.
- TRANSFERDATA: Evaluates measuring value from the ring buffer the last value is given first. OR
- POLL: First in, first out, values are stored in the ring buffer. Function for control and regulation applications.

7.3 Software Gating (Gate) on the Sensor

- DAT_OUT_ON: The digital data output of the measuring values is activated
- TRANSFERDATA: Evaluates measuring values from the ring buffer, delivers the last given value first.
- DAT_OUT_OFF: Deactivates the digital data output of the measuring values.

7.4 Hardware Gating (Gate) on the Sensor

- SET_SYNCMODE/TRIGGERMODE: Set the reaction of the sensor input to low or high level.
- Create the level on the sensor input.
- TRANSFERDATA: Evaluates measuring values from the ring buffer, delivers the last given value first.

This example requires the functionality in the sensor.

7.5 Hardware Gating (Gate) with IF2008

- Data is continuously given by the sensor
- USE_GATE: Opens or blocks the FIFO.
- 5V TTL an IF2008: Data is acquired or blocked.
- CLEAR_BUFFERS: Deletes the ring buffer and the in-output buffer of the IF2008. Therefore, using decaying data is avoided.
- TRANSFERDATA: Evaluates the measuring value from the ring buffer, the last given value is given first.

7.6 Synchronised Measuring ValueEvaluation with Encoder and IF2008

Construction: Sensor on cable 1, encoder on channel 7 (first encoder)

- SensorID = CreateSensorInstance (SENSOR_ILD1700)
- SetParameterString (SensorID, “IP_Interface“,“IF2008“)
- OpenSensor (SensorID)
- SetParameterString (SensorID, “S_Command“,“Get_Settings“)
- SensorCommand (SensorID)

- EncoderID = CreateSensorInstance (PCI_CARD_IF2008)
- SetParameterString (EncoderID, “IP_Interface“,“IF2008“)
- SetParameterInt (EncoderID, “IP_ChannelNumber“, 6)
- OpenSensor (EncoderID)
- SetParameterString (EncoderID, “S_Command“,“Set_EncoderInterpolation“)
- SetParameterInt (EncoderID, “SP_EncoderInterpolation“, 0) // 0 = single evaluation
- SensorCommand (EncoderID)

- SetParameterString (EncoderID, “S_Command“,“Set_EncoderLatchSource“)
- SetParameterInt (EncoderID, “SP_EncoderLatchSource“, 4) //4 = Sensor on channel 1, synchronised evaluation with ILD1700
- SensorCommand (EncoderID)

- SetParameterString (SensorID, “S_Command“,“Clear_Buffers“)
- SetParameterInt (SensorID, “SP_AllDevices“, 1) // 1 = deletes all connected buffers of the unit
- SensorCommand (SensorID)

```
while (running)
 {
        TransferData (SensorID, rawData, scaledData, nbrValues, read)
        TransferData (EncoderID, rawData, scaledData, nbrValues, read)
        …
 }
```

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